

# Direct Observation of Channel Hot-Electron Energy in Short-Channel Metal-Oxide-Semiconductor Field-Effect Transistors

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## ABSTRACT

An experimental method is proposed to extract the channel hot-electron (CHE) energy ( $\varphi_e$ ) in the nano-meter-scaled metal-oxide-semiconductor field-effect transistors (MOSFETs). Accelerated by localized electric field in the drain induced channel depletion region, the CHEs obtain larger kinetic energy than the other unaccelerated channel electrons, and they gain greater probability of tunneling through the gate oxide so as to enlarge the gate leakage current. By monitoring the CHE enhanced gate leakage transients and solving the one-dimensional Schrödinger equation, the reduced gate barrier height ( $\varphi_B$ ) and the  $\varphi_e$  can be extracted. This method is applicable to the short-channel MOSFETs with a channel length less than 150nm with promising accuracy, and it is advantageous owing to its simplicity and timely-applicability to the very recent ultra-small-feature-sized MOSFETs.

## I. INTRODUCTION

CHE energy is one important parameter for design and modeling of short-channel MOSFETs. With unbalanced shrinkage of device dimensions and operating biases, the lateral field from the drain to the source ( $E_{DS}$ ) along the channel of a MOSFET is drastically enlarged, and CHEs are thus increasingly generated. CHEs degrade the gate dielectric ( $\text{SiO}_2$ ) and the semiconductor-oxide ( $\text{Si} / \text{SiO}_2$ ) interface (the channel) during relaxation, bringing about serious reliability degradations<sup>[1-3]</sup>. On the other hand, however, CHE injection is adopted to enable the charge injection for NOR-type Flash memories, and the velocity overshoot induced by the ballistic transport of CHEs<sup>[4]</sup> enhances the operating speed of short-channel MOSFETs and Flash memories. Moreover, the modulation of  $\varphi_e$  is important for achieving accurate threshold voltage ( $V_{th}$ ) control for multi-level cell Flash memories<sup>[5]</sup>. Several methods have been reported to observe  $\varphi_e$  for MOSFETs. For example, spectroscopic experiments were performed to observe the  $\varphi_e$  distribution by detecting CHE induced photon emission<sup>[1]</sup>, and the lateral hot-electron transistors (LHETs) were fabricated for a direct  $\varphi_e$  observation<sup>[2]</sup>. However, it is very difficult to apply these methods to the current nano-meter-scaled MOSFETs due to either

the complicated experimental schemes (photon detection in<sup>[1]</sup>) or the incompatible device structures (LHET in<sup>[2]</sup>). Thus, the Monte-Carlo simulation is usually adopted as an alternative method in the estimation of  $\varphi_e$  distribution<sup>[6]</sup>.

In this study, we propose an electric method for direct extraction of  $\varphi_e$  for the short-channel MOSFETs. With the source ( $V_S$ ) grounded and the inverted channel turned on, drain bias ( $V_D$ ) is applied to boost the channel electrons to be CHEs. The CHEs obtain larger  $\varphi_e$  than the other unaccelerated channel electrons, and they sense a reduced barrier height ( $\varphi_B$ ) of tunneling. As a result, the CHEs obtain greater probability of tunneling through the gate oxide when the gate barrier is shrunk by a gate bias ( $V_G$ ), as shown in Fig. 1(a). By measuring the CHEs enhanced gate leakage current ( $J_G$ ) characteristics and solving the one-dimensional Schrödinger equation, the reduced gate oxide barrier height  $\varphi_B$  and the  $\varphi_e$  can be obtained. This experimental method is simple and valid to the current nano-meter-scaled MOSFETs, and it presents consistent results on the  $\varphi_e$  distribution when compared to the other experimental and computational methods<sup>[1,2,6]</sup>.

## II. THEORY

When the channel is turned on for an *n*-channel MOS transistor, the conduction band ( $\varphi_c$ ) of the Si-substrate is lowered than the Fermi-level ( $\varphi_f$ ) by band bending at the Si-substrate/gate  $\text{SiO}_2$  interface, where the free electrons accumulate to form an inverted channel with a negligible thickness, as shown in Fig. 1(a). The channel electrons are located around  $\varphi_f$ , having an electron energy of  $\varphi_{eo} = k_B T_{eo}$ , where  $k_B$  is the Boltzmann constant, and  $T_{eo}$  is the channel electron temperature under the channel electric field of  $E_{DS} = 0 \text{ MV/cm}$ <sup>[1]</sup>. Under increasing gate electric field  $E_{ox} \approx V_G / D_{ox}$ , where  $D_{ox}$  is the gate oxide thickness, the energy band of the gate oxide undergoes a triangle transformation. The Fowler-Nordheim (F-N) tunneling of electrons occurs when  $E_{ox}$  is at about 6 - 8 MV/cm<sup>[3]</sup>. However, the  $\varphi_e$  of channel electrons is less dependent on  $E_{ox}$ , since  $E_{ox}$  has a negligible accelerating path to the channel electrons along the substrate-gate axis, as shown in Fig. 1(a)<sup>[1,3]</sup>. On the other hand, channel electrons can be effectively accelerated by  $E_{DS}$ , as shown in Fig. 1(b). It was understood that the CHE acceleration occurs at

the pinch-off region under  $E_{acc} \approx (V_D - V_{sat}) / W_{dep}$ , where  $V_{sat}$  is the saturation voltage, and  $W_{dep}$  is the channel depletion width. Being accelerated by  $E_{acc}$ , some channel electrons obtain sufficient energy  $\varphi_e$  to be CHEs, and they induce the CHE enhanced tunneling under  $E_{ox}$ , as shown in Fig. 1(a). The enlarged  $J_G$  is proportional to the channel electron density  $N_{ce}$  and the  $\varphi_e$ -dependent CHE tunneling probability  $[p(\varphi_e)]$ .  $J_G$  can thus be expressed as

$$J_G \propto N_{ce} \cdot p(\varphi_e), \quad (1)$$

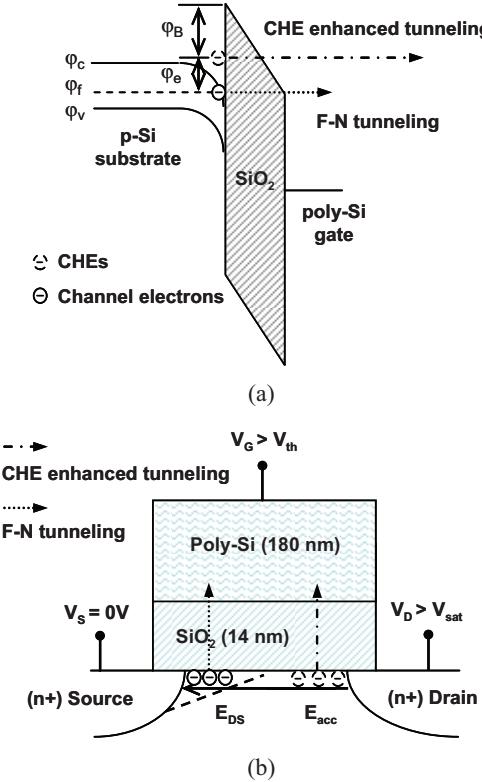


Fig. 1. (a) Band diagram of a MOSFET during F-N tunneling of CHEs. (b) Illustrations of the cross-sectional device structure, the F-N tunneling of the unaccelerated channel electrons along the inverted channel and the enhanced tunneling of CHEs in the drain bias induced substrate depletion (pinch-off) region.

It is understood that  $N_{ce}$  is mainly dependent on  $V_S$  and  $V_G$  after the occurrence of pinch-off<sup>[7]</sup>. Thus, we think that  $N_{ce}$  remains unchanged under a constant  $V_G$  and  $V_S$ , despite the increase of  $V_D$  when  $V_D > V_{sat}$ . In this regard, the  $E_{ox}$  and  $E_{acc}$ -dependent  $J_G$  is mainly affected by  $p(\varphi_e)$ , and it can be expressed as

$$J_G(E_{ox}, E_{acc}) \propto 1.54 \times 10^{-6} (\varphi_B)^{-1} E_{ox}^2 \exp\left[-\frac{6.83 \times 10^7 (\varphi_B)^{3/2}}{E_{ox}}\right], \quad (2)$$

when the electron effective mass approximately equals to

the electron rest mass in SiO<sub>2</sub><sup>[8]</sup>. As the  $E_{ox}$  and  $E_{acc}$  are given, and  $J_G(E_{ox}, E_{acc})$  is measurable, the  $\varphi_B(E_{acc})$  can be extracted by solving equation (2). In MOSFETs with a Si-substrate and a SiO<sub>2</sub> gate barrier,  $\varphi_e = [3.2 - \varphi_B]eV$ <sup>[3]</sup>.

### III. EXPERIMENT AND DISCUSSION

The  $J_G(E_{ox}, E_{acc}) / E_{ox}^2$  versus  $1 / E_{ox}$  characteristics under  $E_{ox} = 0 - 10.0MV/cm$  and  $E_{acc} = 0 - 0.33MV/cm$  obtained from a MOSFET with gate length  $L_G = 100$  nm and  $D_{ox} = 14$  nm are shown in Fig. 2(a). It is understood that the channel electrons accumulate along the Si / SiO<sub>2</sub> interface to form the conducting channel when  $E_{ox} > V_{th} / D_{ox} \approx 1.2MV/cm$ , and they are accelerated by  $E_{acc}$  to be CHEs. The CHEs have greater probability of tunneling through the gate oxide under  $E_{ox} = 5.0 - 10.0MV/cm$  at room temperature.  $J_G(E_{ox}, E_{acc})$  is enhanced, and  $\varphi_B(E_{acc})$  can be extracted by solving equation (2). It is found that  $\varphi_B \approx 2.53eV, 2.58eV, 2.67eV, 2.94eV$ , and  $3.04eV$  under  $E_{acc} = 0.33, 0.27, 0.21, 0.18$ , and  $0MV/cm$ . The linearity of the  $[J_G(E_{ox}, E_{acc}) / \alpha E_{ox}^2]$  versus  $1 / E_{ox}$  under various  $E_{acc}$  supports the credibility of this method, as the slopes of  $\ln[J_G(E_{ox}, E_{acc}) / \alpha E_{ox}^2]$  versus  $1 / E_{ox}$  yield  $(\varphi_B)^{3/2}$ <sup>[8]</sup>. However, the slopes  $[J_G(E_{ox}, E_{acc}) / E_{ox}^2]$  versus  $1 / E_{ox}$  are no longer linear when  $E_{ox} > 8.3MV/cm$  probably due to the disturbance induced by the substrate hot electron (SHE) injection<sup>[3,8]</sup>. Note that the  $\varphi_B$  is obtained to be  $\sim 3.04eV$  between Si / SiO<sub>2</sub> under  $E_{acc} = 0MV/cm$ . This is smaller than the reported value (3.1 - 3.2eV)<sup>[3,8]</sup>. We think that this is induced by the resonant F-N tunneling through the 14-nm-thick gate SiO<sub>2</sub><sup>[9]</sup>. Moreover,  $E_{acc} < 0.33MV/cm$  in this study to avoid the disturbance induced by the drain avalanche hot carrier (DAHC) injection<sup>[3]</sup>.

The  $\varphi_e(E_{acc})$  is converted from  $\varphi_B(E_{acc})$  by  $\varphi_e(E_{acc}) = [3.2 - \varphi_B(E_{acc})]eV$  and plotted versus  $E_{acc}$ , as shown in Fig. 2(b). It is understood that  $\varphi_e(E_{acc})$  essentially obeys the Boltzmann-Maxwell distribution<sup>[1]</sup>. Nevertheless, we think that the non-uniformly distributed  $\varphi_e(E_{acc})$  can be modulated so as to simplify the device modeling. The average  $\varphi_e(E_{acc})$  is independent to the spatial distribution of CHEs along the channel but still affects the device performance. It is found that the  $\varphi_e(E_{acc})$  is proportional to the  $E_{acc}$ . The consistency between  $\varphi_e(E_{acc})$  and  $e(V_D - V_{sat})$  suggests that channel electrons driven by  $E_{acc}$  tend to have a ballistic transport across the  $W_{dep}$ <sup>[4]</sup>. However,  $\varphi_e(E_{acc})$  must be smaller than the work done by  $E_{acc}$  in the  $W_{dep}$ , which is  $e(V_D - V_{sat})$ , due to the Coulomb scattering between the channel electrons and Si lattice during the channel electron acceleration.

This method is applied to MOSFET devices with  $D_{ox} = 14$  nm and  $L_G = 90 - 1000$  nm, and the obtained  $\varphi_e$  under constant  $E_{acc} = 0.33MV/cm$  are plotted versus  $L_G$  in Fig. 2(b). It is found that  $\varphi_e$  decreases from  $0.678eV$  to  $0.272eV$  for devices with  $L_G = 90 - 1000$  nm. We think that the extraction of  $\varphi_e$  is disturbed by the F-N tunneling of channel electrons, as shown in Fig. 1(b). For example,

$W_{\text{dep}} \approx 70$  nm under  $V_D = 3$  V when the doping densities of the Si substrate is  $1 \times 10^{18} \text{ cm}^{-3}$  and that of the lightly-doped-drain-extension is  $2.27 \times 10^{22} \text{ cm}^{-3}$ . With  $V_{\text{sat}} \approx 0.7$  V,  $E_{\text{acc}} \approx 0.33 \text{ MV/cm}$ . When  $L_G = 100$  nm,  $J_G$  is dominated by the CHE tunneling in the  $W_{\text{dep}}$  region. However, with larger  $L_G$ , e.g., 1000 nm,  $J_G$  is dominated by the tunneling of channel electrons in the region between the  $W_{\text{dep}}$  and the source, as shown in Fig. 1(b). Therefore, the obtained  $\varphi_e$  diverges from the CHE energy for the long-channel MOSFETs. It is understood that this method is valid for the MOSFETs with a  $L_G \leq 150$  nm, as shown in Fig. 2(b).

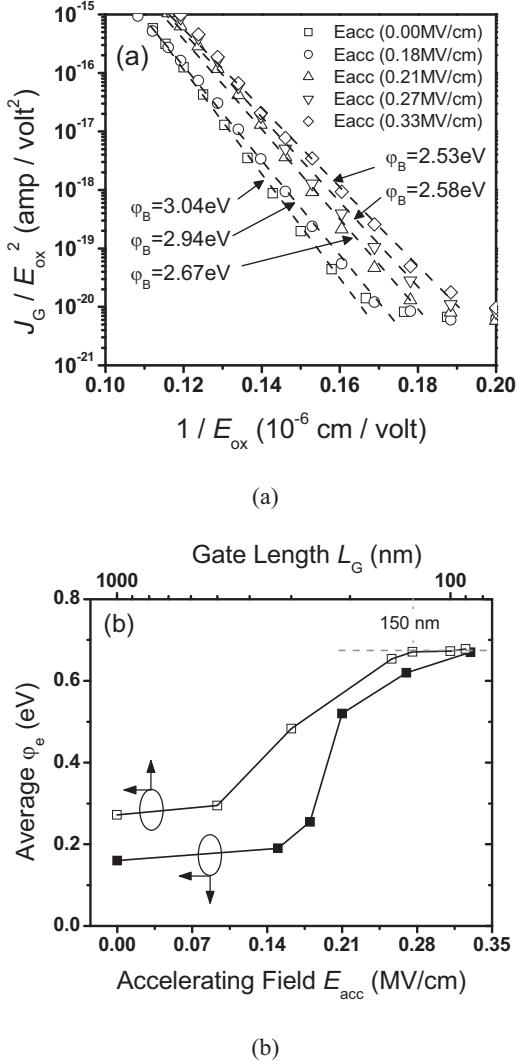


Fig. 2. (a) CHE enhanced gate leakage versus the gate electric field  $E_{\text{ox}}$  for a MOSFET with  $L_G = 100$  nm under  $E_{\text{acc}} = 0 - 0.33$  MV/cm. (b) The extracted CHE energies under various  $E_{\text{acc}} = 0 - 0.33$  MV/cm and  $L_G = 90 - 1000$  nm.

The technical features and  $\varphi_e$  obtained by this method and the other methods are listed in Table 1. The consistent results support the validity of this proposed method.

Table 1. The technical features and the obtained results by using this method and the other methods

References	This study	[1] T-ED 34 (7), pp. 1501 - 1508, 1987	[2] APL 75 (8), pp. 1113 - 1115, 1999	[6] T-ED 35 (8), pp. 1344 - 1350, 1988
Experimental setup	Electrical	Optical & electrical	Electrical	Computational
Valid device structure	MOSFET	MOSFET	LHET	MOSFET
Valid device dimension	$L_G \leq 150$ nm	$L_G \sim \mu\text{m}$	$L_G \approx 100$ nm	$L_G \sim \mu\text{m}$
Channel structure	Continuous $n$ -channel	Continuous $n$ -channel	Split $n$ -channel	-
Mechanism	CHE enhanced F-N tunneling	CHE induced photo emission	CHE enhanced drain current	Theoretical calculation
Estimated CHE energy	$\sim 0.7$ eV under $E_{\text{acc}}$ of 0.30 MV/cm	$\sim 0.2 - 0.3$ eV under $E_{\text{acc}}$ of $\sim 0.4$ MV/cm	$\sim 0.7$ eV under emitter bias ( $V_D$ ) of 1.04 V	$\sim 0.8 - 1.0$ eV under $E_{\text{acc}}$ of $\sim 0.4$ MV/cm
Capability of estimating the CHE spatial distribution	Approximate	Approximate	No	Yes

#### IV. CONCLUSION

In this study, an experimental method is proposed to extract the CHE energy  $\varphi_e$  for short-channel MOSFETs. By monitoring the CHE enhanced gate leakage transient and solving the Schrödinger equation, the reduced barrier height  $\varphi_B$  and the  $\varphi_e$  are estimated. This method is valid for the short-channel MOSFETs with a  $L_G \leq 150$  nm.

#### REFERENCES

- [1] A. Toriumi, M. Yoshimi, M. Iwase, Y. Akiyama, and K. Taniguchi, "A study of photon emission from  $n$ -channel MOSFET's," *IEEE Trans. Electron Devices*, vol. 34, no. 7, pp. 1501-1508, 1987.
- [2] T. Sakamoto, H. Kawaura, T. Baba, and T. Iizuka, "Direct observation of hot-electron energy distribution in silicon metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 75, no. 8, pp. 1113-1115, 1999.
- [3] E. Takeda, C.Y. Yang, and A.K. Miura-Hamada, *Hot Carrier Effects in MOS Devices*, New York, 1995.
- [4] T. Mizuno, R. Ohba, and K. Ohuchi, "Velocity overshoot greater than  $10^7$  cm/s at room temperature in sub-0.1- $\mu\text{m}$  silicon-on-insulator devices," *Appl. Phys. Lett.*, vol. 69, no. 1, pp. 106-108, 1996.
- [5] G. Zhang, W.S. Hwang, M.B. Santosh, S.-H. Lee, B.J. Cho, and W.J. Yoo, "Novel  $\text{ZrO}_2/\text{Si}_3\text{N}_4$  dual charge storage layer to form step-up potential wells for highly reliable multi-level cell Flash memory application," in *IEDM Tech. Dig.*, 2007, s4p3, pp. 83-86.
- [6] K. Kato, "Hot-carrier simulation for MOSFET's using a high-speed Monte Carlo method," *IEEE Trans. Electron Devices*, vol. 35, no. 8, pp. 1344-1350, 1988.
- [7] S. Dimitrijev, *Understanding Semiconductor Devices*, New York: Oxford Univ. Press, 2000.
- [8] E.H. Snow, "Fowler-Nordheim tunneling in  $\text{SiO}_2$  films," *Solid State Communications*, vol. 5, no. 10, pp. 813-815, 1967.
- [9] A. Korotkov and K. Likharev, "Resonant Fowler-Nordheim tunneling through layered tunnel barrier and its possible applications," in *IEDM Tech. Dig.*, 1999, pp. 223-226.