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Enhanced electrodynamic gating in two-dimensional transistors using ferroelectric capping

Hemendra Nath Jaiswal[1], **Maomao Liu**[1], **Simran Shahi**[1], **Anthony Cabanillas**[1], **Sichen Wei**[2], **Yu Fu**[2], **Anindita Chakravarty**[1], **Asma Ahmed**[1], **Joel Muhigirwa**[1], **Fei Yao**[2,*] and **Huamin Li**[1,*]

[1] Department of Electrical Engineering, University at Buffalo, The State University of New York, Buffalo, NY, 14260, United States of America

[2] Department of Materials Design and Innovation, University at Buffalo, The State University of New York, Buffalo, NY, 14260, United States of America

* Authors to whom any correspondence should be addressed.

E-mail: feiyao@buffalo.edu **and** huaminli@buffalo.edu

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Abstract

Two-dimensional (2D) materials such as semiconductors and ferroelectrics are promising for future energy-efficient logic devices because of their extraordinary electronic properties at atomic thickness. In this work, we investigated a van der Waals heterostructure composited of 2D semiconducting MoS_2 and 2D ferroelectric $CuInP_2S_6$ (CIPS) and $NiPS_3$. Instead of using 2D ferroelectrics as conventional gate dielectric layers, here we applied CIPS and $NiPS_3$ as a ferroelectric capping layer, and investigated a long-distance coupling effect with the gate upon the sandwiched 2D MoS_2 channels. Our experimental results showed an outstanding enhancement of the electrodynamic gating in 2D MoS_2 transistors, represented by a significant reduction of subthreshold swing at room temperature. This was due to the coupling-induced polarization of 2D ferroelectrics at 2D semiconductor surface which led to an effective and dynamic magnification of the gate capacitance. Meanwhile, the electrostatic gating was remained steady after adding the ferroelectric capping layer, providing ease and compatibility for further implementation with existing circuit and system design. Our work demonstrates the long-distance coupling effect of 2D ferroelectrics in a capping architecture, reveals its impacts from both electrodynamic and electrostatic perspectives, and expands the potential of 2D ferroelectrics to further improve the performance of energy-efficient nanoelectronics.

Introduction

To achieve continued scaling down of field-effect transistors (FETs), new classes of semiconductors which are immune to short-channel effects are highly desired, because the performance of existing Si FETs degrades severely within sub-5 nm gate length [1]. Another roadblock for existing FETs is the Boltzmann tyranny which defines the inability of supply voltage to be further suppressed [2–4]. In conventional FETs, the switching mechanism is governed by thermionic emission and described by subthreshold swing (SS),

$$SS = \left[\frac{d(\log J_D)}{dV_G}\right]^{-1} = \frac{dV_G}{d\varphi_{ch}} \cdot \frac{d\varphi_{ch}}{d(\log J_D)} = m \cdot n \quad (1)$$

Here J_D (or I_D) is the drain current density (or drain current), V_G is the gate voltage, and φ_{ch} is the channel potential energy. $m = dV_G/d\varphi_{ch}$ is the body factor indicating the capacitive gating efficiency, and $n = d\varphi_{ch}/d(\log J_D)$ is the transport factor representing the charge transport efficiency. SS, as a product of the body factor and transport factor, fundamentally sets a physical limit at 60 mV/decade at room temperature, and consequently constrains further improvement of the energy efficiency for transistor operation.

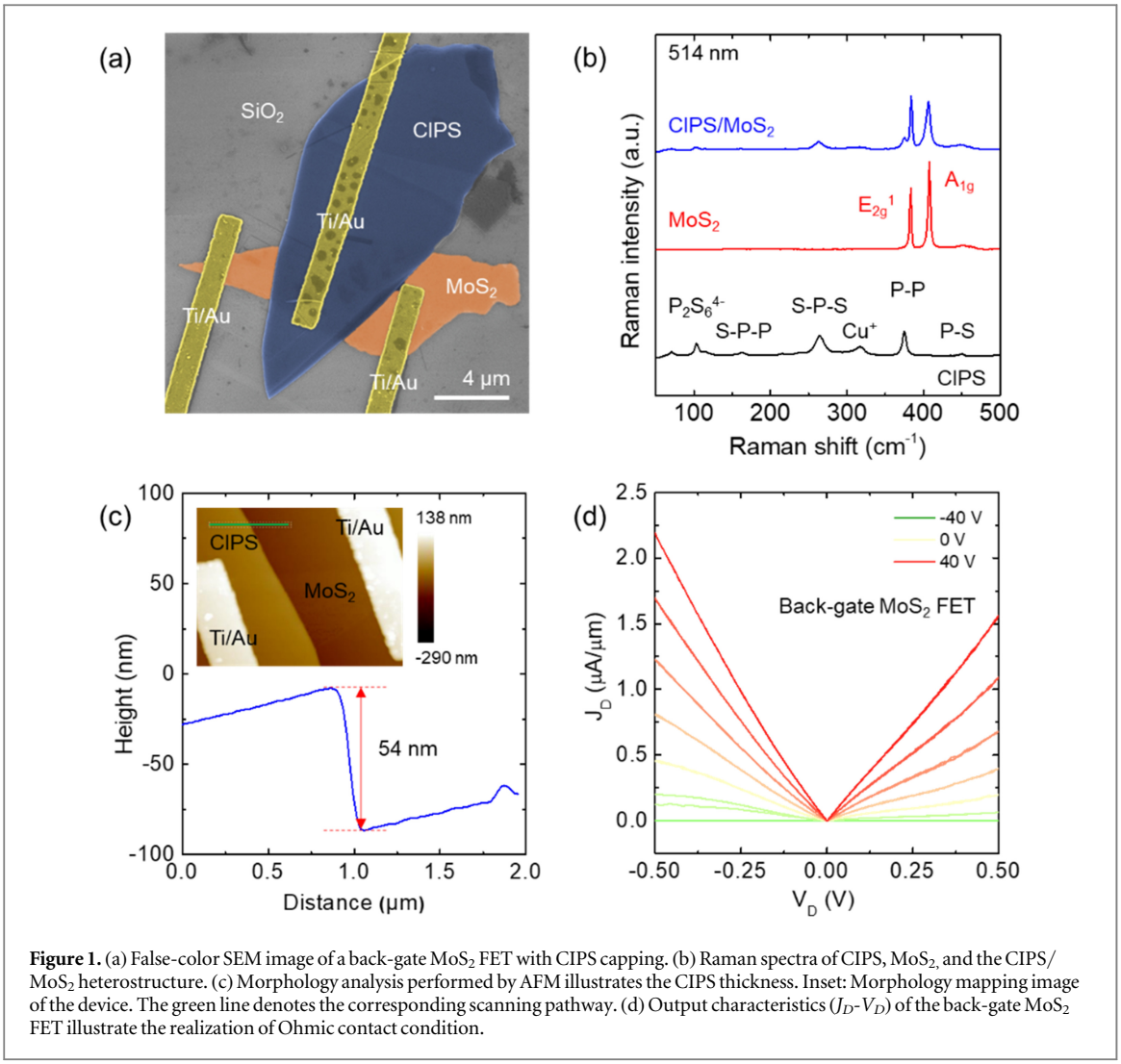

Figure 1. (a) False-color SEM image of a back-gate MoS_2 FET with CIPS capping. (b) Raman spectra of CIPS, MoS_2, and the CIPS/MoS_2 heterostructure. (c) Morphology analysis performed by AFM illustrates the CIPS thickness. Inset: Morphology mapping image of the device. The green line denotes the corresponding scanning pathway. (d) Output characteristics (J_D-V_D) of the back-gate MoS_2 FET illustrate the realization of Ohmic contact condition.

With the rise of two-dimensional (2D) graphene [5], new FET concepts based on 2D van der Waals (vdW) materials and their hetero-structures have been demonstrated, which are free from the short-channel effects and capable of reaching sub-60 mV/decade SS [6–11]. Especially, 2D ferroelectric materials such as $CuInP_2S_6$ (CIPS) and $NiPS_3$ have shown great potential to realize a variety of energy-efficient logic devices [12–14], for example, negative capacitance FETs [4, 15–17] and ferroelectric FETs [18, 19]. In these prototypes, 2D ferroelectrics and 2D semiconductors are stacked vertically to form a heterostructure, and the interlayer vdW interaction resolves lattice mismatch at the hetero-interfaces. 2D ferroelectrics, in general, serve as a gate dielectric sandwiched by a metal gate and 2D semiconductor channel, and provides the gate capacitance to modulate charge density in 2D semiconductor channel. Being different from conventional dielectrics such as 2D *h*-BN or three-dimensional (3D) high-*k* dielectrics, 2D ferroelectrics possess spontaneous polarization states in the absence of an electric field, and enables the polarization switching between these states in response to an applied external electric field.

In this work, we investigated a novel architecture based on 2D semiconducting MoS_2 and 2D ferroelectric CIPS and $NiPS_3$. Here CIPS and $NiPS_3$ were exploited as a ferroelectric capping layer in gate/dielectric/2D semiconductor/2D ferroelectric heterostructures, in comparison with the role as a gate ferroelectric layer in conventional gate/2D ferroelectric/2D semiconductor heterostructures. A long-distance coupling effect was identified between the gate and 2D ferroelectrics, even across around 300 nm-thick dielectric and 2D semiconductor layers. Owing to this strong ferroelectric coupling effect, an outstanding enhancement of the electrodynamic gating on 2D MoS_2 channel was realized, which was represented by a significant reduction of SS at room temperature (averagely from 1 to 0.2 V/decade for multiple devices) and quantitatively described by an effective improvement of *m* (by a factor of ~5). In contrast to the outstanding enhancement of the electrodynamic gating, the electrostatic gating, featured by on-states current density, transconductance, and on/off ratio, were remained steady after adding the ferroelectric capping layer, suggesting the ease and compatibility

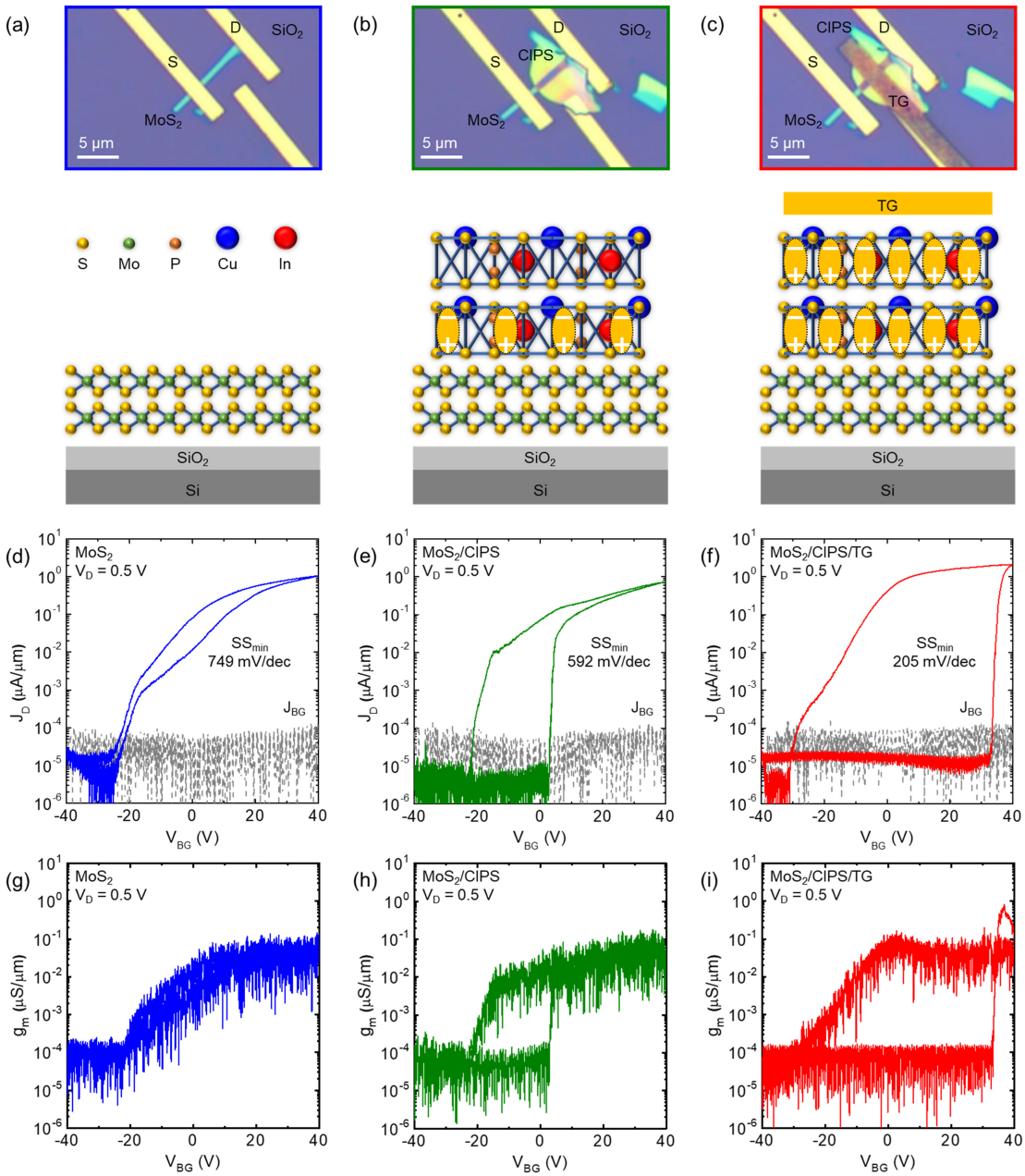

Figure 2. (a)–(c) Microscopy images (top panel) and cross-section schematics (bottom panel) of the back-gate MoS_2 FETs with different gating conditions, including (a) the MoS_2 channel without the CIPS capping layer, (b) the MoS_2 channel with the CIPS capping layer, exhibiting weak polarizations, and (c) the MoS_2 channel with the CIPS capping layer and a TG metal layer, exhibiting strong polarizations. (d)–(f) Room-temperature J_D-V_{BG} transfer characteristics for each device configuration. J_{BG} is the leakage current density monitored from the BG electrode. (g)–(i) The corresponding g_m-V_{BG} characteristics for each device configuration.

for further implementation of this technique with existing circuit and system design. Our work demonstrates the long-distance coupling effect of 2D ferroelectrics in a capping architecture, reveals its impacts from both electrodynamic and electrostatic perspectives, and expands the potential of 2D ferroelectrics to further improve the performance of energy-efficient nanoelectronics.

Experiments

We fabricated multiple dual-gate FETs using mechanically exfoliated MoS_2, CIPS, and $NiPS_3$ flakes. Firstly, MoS_2 flakes were placed on Si substrate (0.01–0.05 Ω cm, as a global back gate, BG), acting as an n-type semiconductor channel to form a typical back-gate thin film transistor. A 285 nm-thick SiO_2 layer, formed by dry chlorinated thermal oxidization, serves as the back-gate dielectric. Source (S) and drain (D) electrodes were patterned by electron beam lithography and deposited with Ti/Au (10 nm/100 nm). Secondly, CIPS or $NiPS_3$

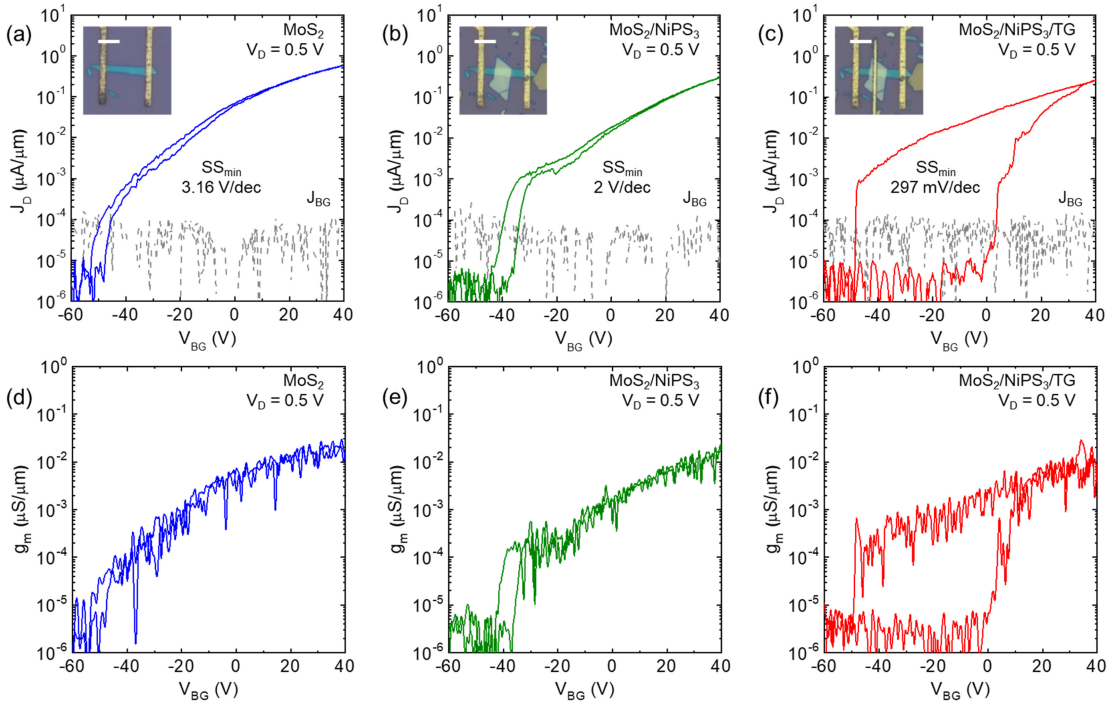

Figure 3. (a)–(c) Room-temperature J_D-V_{BG} transfer characteristics of the back-gate MoS_2 FETs with different gating conditions, including (a) the MoS_2 channel without the $NiPS_3$ capping layer, (b) the MoS_2 channel with the $NiPS_3$ capping layer, and (c) the MoS_2 channel with the $NiPS_3$ capping layer and a TG metal layer. Inset: The corresponding microscopy images for each device configuration. Scale bar: 5 μm. (d)–(f) The corresponding g_m-V_{BG} characteristics for each device configuration.

flakes were transferred on top of MoS_2, acting as a ferroelectric capping layer. Thirdly, a top gate (TG) electrode, deposited with Ti/Au (10 nm/100 nm), was added to complete the top gate/2D ferroelectric/2D semiconductor/SiO_2/Si stacking structure. Therefore, three types of back-gate FET and one type of top-gate FET configurations can be realized with the common channel and source/drain contacts, including (i) the back-gate MoS_2 FET with SiO_2 dielectric, (ii) the back-gate MoS_2 FET with SiO_2 dielectric and CIPS (or $NiPS_3$) capping, (iii) the back-gate MoS_2 FET with SiO_2 dielectric, CIPS (or $NiPS_3$) capping, and the TG metal plate, (iv) and the top-gate MoS_2 FET with CIPS (or $NiPS_3$) ferroelectric. Due to the shared channel and S/D/BG contacts, the difference in their performance can be attributed to the disparate electrostatic and electrodynamic gating conditions.

As an example, a completed dual-gate FET device using MoS_2 and CIPS is shown in figure 1(a). Both MoS_2 and CIPS were verified by Raman spectroscopy and energy dispersive spectroscopy (EDS), and the thicknesses were measured by atomic force microscopy (AFM), as shown in figures 1(b) and (c) as well as figure. S1 and S2. Similar characterization was also performed on the device with $NiPS_3$, as shown in figure. S3. With a grounded source, drain current (J_D) as a function of drain voltage (V_D), back-gate voltage (V_{BG}), and top-gate voltage (V_{TG}) were measured by a semiconductor parameter analyzer and a vacuum probe station. Room-temperature output characteristics (J_D-V_D) show good linearity at low V_D, suggesting the formation of an Ohmic contact condition [20, 21], as shown in figure 1(d). Transfer characteristics (J_D-V_{BG} and J_D-V_{TG}) were measured to evaluate electrostatic and electrodynamic gating for each FET configuration, which will be discussed in detail.

Results and discussion

With the same MoS_2 channel and electrode contacts, three back-gate FET configurations are compared to elucidate the impact of ferroelectric capping on transistor performance. Starting from a back-gate MoS_2 FET, a CIPS flake is added to cap the channel, and then a metal TG is added on top of CIPS. Microscopy images and cross-section schematics for each configuration are shown in figures 2(a)–(c). The minimum SS (SS_{min}), extracted from J_D-V_{BG} transfer characteristics [22, 23], equals 749, 592, and 205 mV/decade, respectively, as shown in figures 2(d)–(f). The corresponding back-gate transconductance, defined as $g_m = dJ_D/dV_{BG}$, is also shown in figures 2(g)–(i) as well as in figure. S4 for each configuration. First, the electrodynamic gating, represented by SS, is significantly enhanced with the CIPS capping in the channel. A gate-induced long-distance coupling is established between the Si BG and CIPS capping layer, introducing polarizations at the

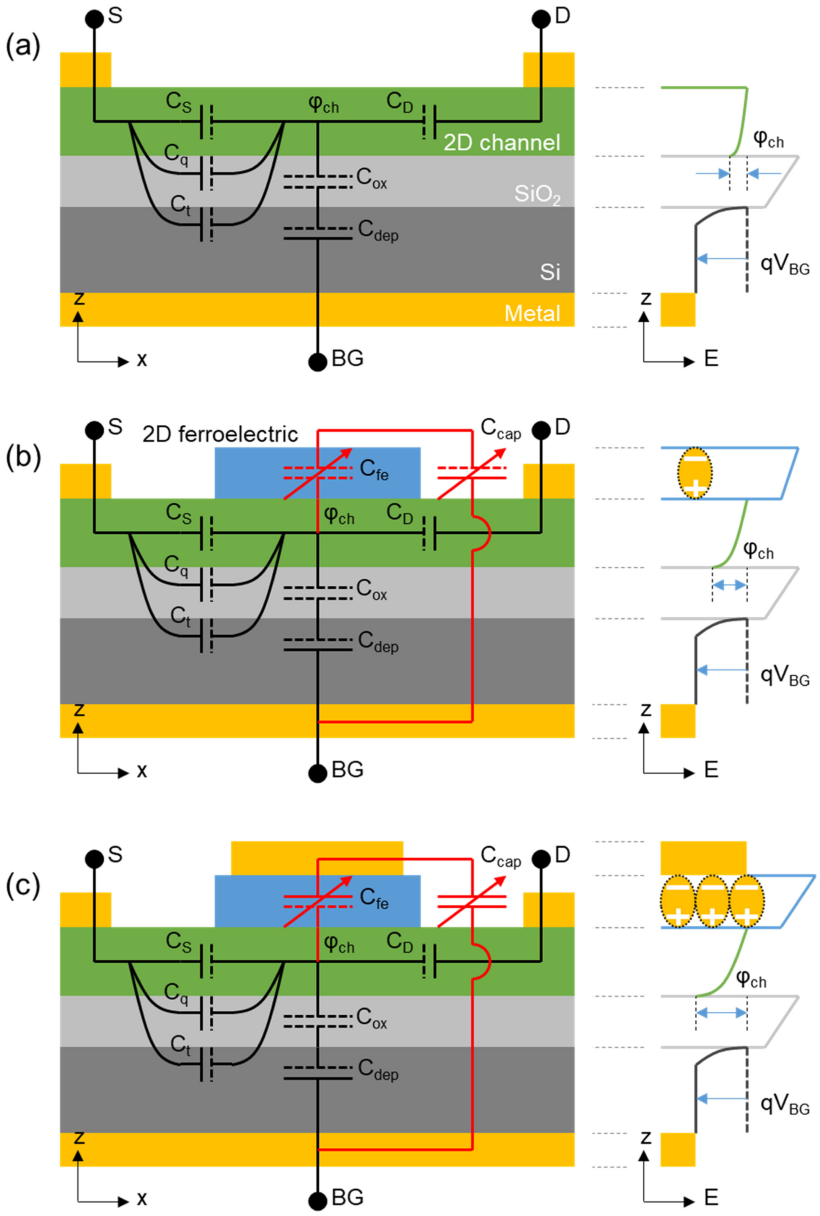

Figure 4. (A) capacitor network model (left) and the corresponding energy band diagram (right) along the gate stack to compare the coupling effect with ferroelectric capping for different device architectures, including (a) a typical back-gate 2D FET without the ferroelectric capping, (b) a back-gate 2D FET with a ferroelectric capping layer, and (c) a back-gate 2D FET with a ferroelectric capping layer and a metal plate. For the same V_{BG} variation, stronger φ_{ch} modulation can be realized with the electrodynamic coupling.

CIPS surface next to the MoS_2 channel. Second, TG as a metal plate on top of the CIPS capping layer can further improve the electrodynamic coupling effect with the Si BG. The metal plate promotes more polarization states in CIPS, attracts more charge carriers in MoS_2 to respond to the BG sweeping, and consequently enhances the coupling-induced electrodynamic gating. Third, the introduction of the CIPS capping layer, either with or without the TG metal plate, only boosts the electrodynamic gating within the switching (subthreshold) regime. For the off state (free of charges in the channel, for example, at $V_{BG} = -40$ V) and the on state (full of charges in the channel, for example, at $V_{BG} = 40$ V), the device is dominated by the electrostatic gating. The CIPS capping has negligible impacts on the electrostatic gating, which can be observed from the consistent J_D ($\sim$1 μA μm^{-1} at the on state), g_m ($\sim$2 μS μm^{-1} at the on state), and on/off ratios ($\sim 10^5$) as compared the reference device without the CIPS capping layer. Fourth, an enlarged hysteresis window is obtained after adding the CIPS capping layer. Similar behavior has been reported for a top-gating structure where CIPS serves as a gate dielectric [19]. As a function of the applied V_{BG}, this ferroelectric hysteresis loop originates from a capacitance matching between the CIPS capacitance and other capacitance in the device architecture. Ideally the hysteresis can be eliminated for logic device applications by operating the ferroelectric-gated FET as a negative capacitance FET. Moreover, the hysteresis-induced distinct on/off ratio

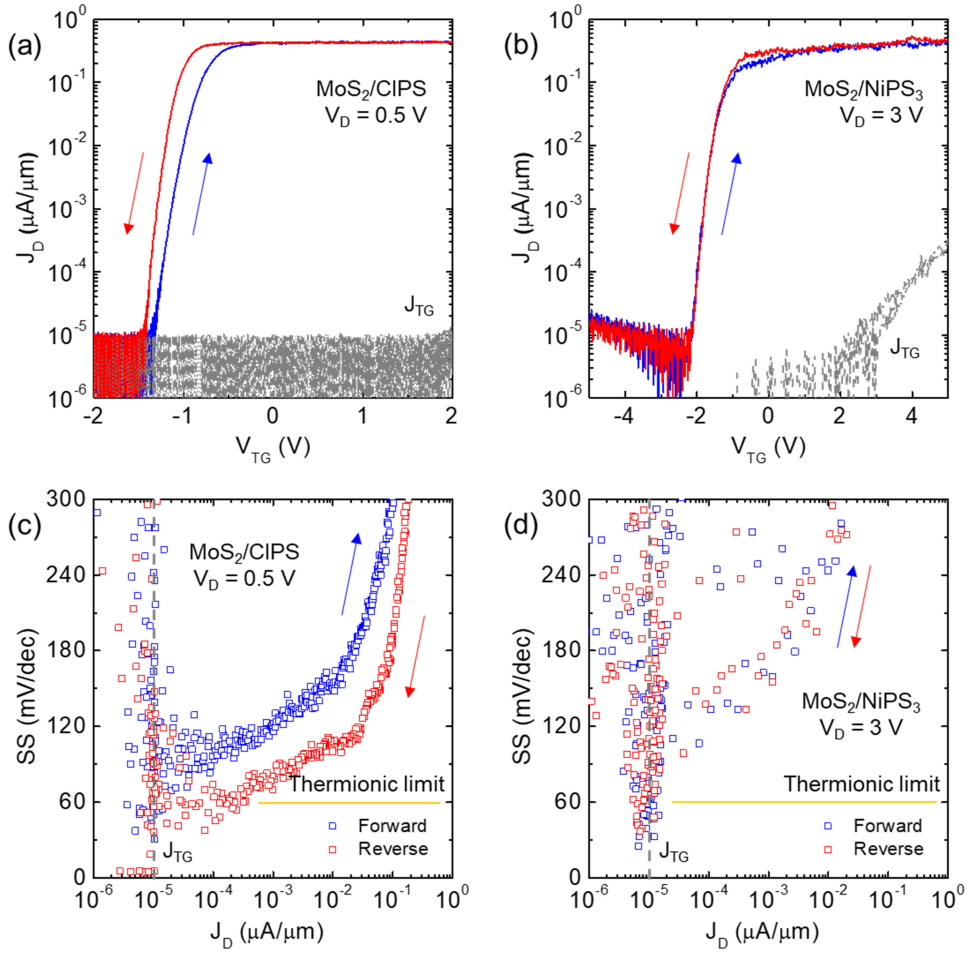

Figure 5. (a), (b) Room-temperature J_D-V_{TG} transfer characteristics of the top-gate MoS_2 FETs with (a) CIPS dielectric and (b) $NiPS_3$ dielectric. J_{TG} is the leakage current density monitored from the TG electrode. (c), (d) The corresponding SS-J_D characteristics for each device configuration. Yellow line denotes the thermionic limit of SS at 60 mV/decade.

between the low and high resistance states (e.g., ~10^5 in this work) can be beneficial for nonvolatile resistive random-access memory (ReRAM) applications. In contrast to the understanding of ferroelectric and negative capacitance FET [18, 19, 24–27] and ReRAM [28–31] devices, further exploration about the hysteresis in the ferroelectric capping structure is needed, such as its dependence on the sweep range, sweep rate, capacitance matching, and prototype demonstrations.

Similarly, we investigate the back-gate MoS_2 FETs with the $NiPS_3$ capping layers at room temperature, and the electrical characterizations are shown in figure 3 as well as in figure. S5. SS_{min} is reduced from 3.16 to 2 V/decade as the $NiPS_3$ capping layer is added to introduce the weak polarizations through the coupling effect. Then the value is drastically decreased to 0.297 V/decade as the TG metal plate is added to enable the strong polarizations. In contrast, J_D, g_m, and on/off ratio are consistent among different configurations, suggesting the immunity of electrostatic gating from the ferroelectric coupling. Key performance metrics of MoS_2 FETs with a variety of the CIPS and $NiPS_3$ capping configurations are summarized in Table S1. These common features observed in both the CIPS- and $NiPS_3$-capped MoS_2 FETs also evidence that the enhanced electrodynamic gating is not attributed to a specific ferroelectric material, but is resulting from the ferroelectric capping architecture and the induced long-distance coupling effect.

To better understand the enhanced electrodynamic gating with the ferroelectric capping, a capacitor network model is developed, as shown in figure 4. Along the gate stack, C_{fe}, C_{ox}, and C_{dep} are the capacitance of the ferroelectric capping layer, SiO_2 dielectric layer, and Si depletion layer, respectively. Along the channel direction, C_q is the quantum capacitance representing the variation of charge density in response to the modulation of φ_{ch}. C_S and C_D describe the capacitive coupling from S and D, respectively. C_t is the capacitance induced by the charge traps involved in charge transport. C_{cap} indicates the capacitive coupling with the Si BG when the ferroelectric capping layer is added [32]. For each type of capacitor, solid and dash lines denote the interfaces with and without metal electrodes, respectively [16]. Due to the involved polarization states, a variable capacitor symbol and red circuits are adopted to represent the electrodynamic response of C_{fe} and C_{cap}, in

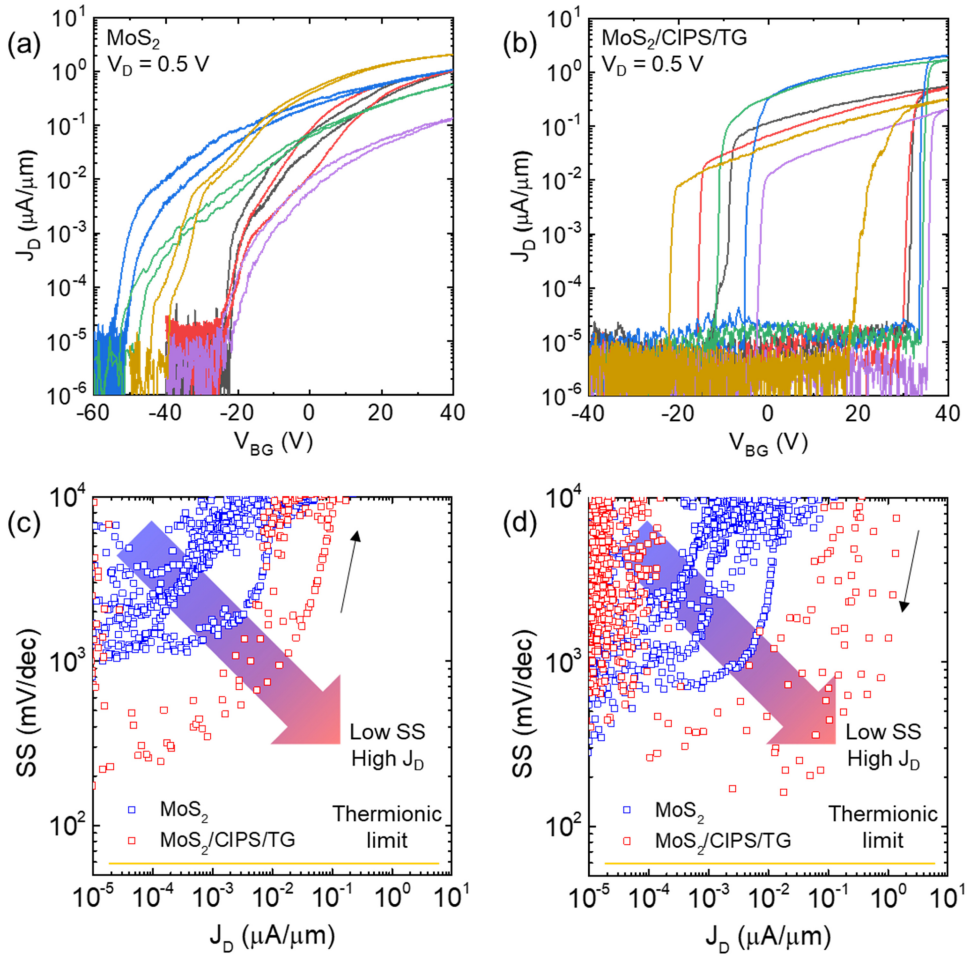

Figure 6. (a), (b) Summary of room-temperature J_D-V_{BG} transfer characteristics of the back-gate MoS_2 FETs, 6 in total, before and after adding a CIPS capping layer and a TG metal plate. (c), (d) The corresponding SS-J_D characteristics in forward and backward sweeps. Yellow line denotes the thermionic limit of SS at 60 mV/decade. The blue-red arrow indicates an overall improvement towards the desired low-SS and high-J_D operation.

contrast with the electrostatic network as marked in black. Meanwhile, the corresponding energy band diagram along the gate stack is illustrated for each device configuration. For the same V_{BG} variation, the ferroelectric capping layer and its coupling effect with BG would lead to a stronger modulation on φ_{ch}. The involvement of the metal plate can further promote the polarizations and coupling effect, enabling an even stronger response of the φ_{ch} variation.

To compare with the conventional architecture in which the ferroelectric layer is sandwiched by the channel and gate, we also evaluate the switching performance of the top-gate MoS_2 FETs using both CIPS and $NiPS_3$ ferroelectrics. The J_D-V_{TG} transfer characteristics at room temperature are shown in figures 5(a) and (b), and the corresponding SS as a function of J_D is shown in figures 5(c) and (d). The ferroelectrics in the top-gate FET structures enable good J_D (~0.4 μA μm^{-1} at the on state) and on/off ratio (~4×10^4), which are comparable with the back-gate FET structure using SiO_2 dielectric. SS_{min} with CIPS is approaching the thermionic limit at 60 mV/decade, and the one with $NiPS_3$ is also close to 100 mV/decade. This superior switching behavior is mainly due to two reasons. First, the ferroelectric layer has a much smaller thickness (~50 nm for both CIPS and $NiPS_3$ flakes) in the top-gate structure, compared to 285 nm-thick SiO_2 dielectric in the back-gate structure. The narrower separation between the gate and channel leads to a higher capacitance according to a parallel-plate capacitor model, and reduces SS close to the thermionic limit. Second, the polarization states in the ferroelectric layer contribute to a magnified capacitance or even a transient negative-capacitance response, which may achieve the sub-thermionic SS. It is rational to anticipate that the benefits of the ferroelectric capping architecture will be enhanced accordingly as the gate dielectric (i.e., 285 nm-thick SiO_2 dielectric in this work) is scaled down, since the corresponding coupling effect and thereby the electrodynamic gating will be promoted as well. Further investigation is needed to explore the upper limit of the ferroelectric capping technique with the extremely miniaturized gating structures.

Moreover, we fabricate and test multiple devices to demonstrate the reproducibility and reliability of the coupling effect through the ferroelectric capping. With 6 devices in total, it is clearly shown that the electrodynamic switching behavior of all the back-gate MoS_2 FETs has been significantly improved after adding the CIPS capping layer and metal plate, while the electrostatic on-state J_D and on/off ratio can be remained steadily, as shown in figures 6(a) and (b). To quantitively evaluate the improvement of the electrodynamic gating, SS as a function of J_D for all the devices are composed as shown in figures 6(c) and (d). For both forward sweeping (from –40 to 40 V) and backward sweeping (from 40 to –40 V), the switching metrics are considerably shifted towards the desired direction to enable the low-SS and high-J_D operation. Specifically, SS_{min} is averagely suppressed from 1 to 0.2 V/decade, even with 285 nm-thick SiO_2 dielectric used in the transistor structure. Owing to the identical channel and metal contacts, the SS improvement can be completely attributed to the enhanced electrodynamic gating which is quantitatively described by m and reduced by a factor of ~5. It is rational to anticipate that, with an extremely miniaturized device architecture, the electrodynamic enhancement induced by the ferroelectric capping will be more effective.

Conclusions

In this work, we significantly improved the switching efficiency of back-gate 2D transistors using a simple 2D ferroelectric capping layer. Owing to a strong and long-distance coupling effect between the gate and the ferroelectric capping layer, the electrodynamic gating on 2D channel can be notably enhanced, giving rise to the improved body factor and thereby SS by a factor of ~5. Whereas the electrostatic gating was remained steady, which provides great compatibility with existing circuit and system designs. Our work demonstrates a novel approach to adopt 2D ferroelectrics in contrast to the conventional understanding, and paves a way to explore the full potential for future energy-efficient nanoelectronics.

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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Author contributions

F Yao and H Li conceived and supervised the project. H N Jaiswal performed the device fabrication and measurement. M Liu, S Shahi, A Cabanillas, A Chakravarty, A Ahmed, and J Muhigirwa participated in the sample preparation and data analysis. S Wei, and Y Fu performed the material characterization.

Conflicts of interest

The authors declare no competing financial interest.

ORCID iDs

Fei Yao https://orcid.org/0000-0001-8414-7955
Huamin Li https://orcid.org/0000-0001-7093-4835

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