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Self-Assembled Wire Arrays and ITO Contacts for Silicon Nanowire Solar Cell Applications

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Self-assembly of silicon nanowire (SiNW) arrays is studied using SF_6/O_2 plasma treatment. The self-assembly method can be applied to single- and poly-crystalline Si substrates. Plasma conditions can control the length and diameter of the SiNW arrays. Lower reflectance of the wire arrays over the wavelength range 200–1100 nm is obtained. The conducting transparent indium-tin-oxide (ITO) electrode can be fully coated on the self-assembled SiNW arrays by sputtering. The ITO-coated SiNW solar cells show the same low surface light reflectance and a higher carrier collection efficiency than SiNW solar cells without ITO coating. An efficiency enhancement of around 3 times for ITO coated SiNW solar cells is demonstrated via experiments.

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Recently, nanostructure (such as nanospheres,[1] nanowire[2–7] or nanopillar[8]) solar cells have been suggested as promising candidates for solar energy harvesting. Silicon is still the leading material used in today's photovoltaic (PV) industry. As the process matures, silicon nanowire (SiNW) or silicon nanopillar (SiNP) structrues have naturally become the focus of nanowire solar cells. However, SiNW solar cells have major drawbacks, such as low carrier collection efficiency[2,5–9] with the larger surface recombination. Fabricated nanowire arrays can not easily be coated by a transparent electrode. As a result, radial p-i-n,[6] tandem p-i-n^+-p^+-i-n[7] and poly-SiNW[9] solar cells may show conversion efficiencies of 3.4%, 4.3% and 4.73%, respectively. In order to enhance conversion efficiency, it is important that the SiNW solar cells have a carrier collection structure. Platinum nanoparticle decorated silicon nanowires have an effective carrier collection structure and have yielded an efficiency of 8.14% for Peng *et al.*[10] To increase efficiency, further research on carrier collection structures is both possible and necessary. In addition, nanostructured solar cells made using low-cost materials are expected to be used in industry. Poly-crystalline nanowire array solar cells are expected to enhance solar cell efficiency despite their very low material cost due to their enlarged p-n junction area and suppressed light reflection. In this work, polycrystalline nano-wire arrays are designed and fabricated using a self-assembly method, which can be formed into a radial p-n junction with full indium-tin-oxide (ITO) coating. The ITO-coated poly-SiNW solar cell has a very large surface area but a short carrier collection path, therefore enhancing light trapping as well as increasing carrier collection efficiency. Thus, a significant enhancement in conversion efficiency is obtained for ITO-coated SiNW solar cells compared to those without ITO coating. The designed structure is promising for future high efficiency nano-wire solar cell applications.

An inductively coupled plasma (ICP) reactor is used for the plasma treatments. The plasma source is controlled by electrical power up to 1500 W, while the sample chuck is independently biased up to 500 W. The source power, rf-bias power, O_2/SF_6 gas ratio, gas flow rate, chamber gas pressure and the etching time can be controlled to self-assemble the nanowire arrays.[11] The experiments are conducted in noncryogenic conditions dependent on the water cooling of the sample chuck (about 293 K). Both single- and poly-crystalline silicon substrates are studied in our experiment. Figures 1(a) and 1(b) show the scanning electron microscopy (SEM) cross-section images of the self-assembled nanowire arrays formed by plasma etching single- and poly-crystalline silicon substrates. From Figs. 1(a) and 1(b), the vertical nanowire arrays were self-assembled on even and uneven surfaces. The width of the poly-crystalline silicon pyramidal structure is about 3 μm, while the diameter of the self-assembled nanowire is only 50–400 nm, which is much less than the width of the uneven surface structure. The self-assembled nanowire array formation mechanisms on both the even and uneven surfaces are believed to be the same. In the case of the uneven surface, the schematic diagram of the self-assembly mechanism is shown in the inset of Fig. 1(c). In the beginning, the plasma-treated surface is mound-shaped.

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The diameter of the hills (50–400 nm) is much less than the width of the uneven surface structure. Drotar *et al.*[12] have proposed that the etching species, e.g. F*, conducted by the substrate-bias and rf-bias power, do not stick on the surface on their first approach, but are reemitted and only stick on the subsequent reemission. As a result, etching species (such as F*) stick much less on the hills of the surface than in the valleys. In the SF_6/O_2 plasma, SF_6 is the source of the active fluorine radicals F* that etch silicon while O_2 is the source of the active oxygen radicals O* that passivate the etched silicon surface. On the hills, F* sticks less and O* passivates the surface. As a result, it is easier for the Si surface to be mound shaped. As time increases further, the roughness of the surface increases and the structure of the formed surface becomes more anisotropic. We think that when F* radicals come into contact with the surface, most of them undergo subsequent reemission so as to stick to the valleys of the structures. When the structure is near vertical, i.e., anisotropic, fewer and fewer F* radicals stick to the sidewall of the structure, the passivation effect of the O* radicals is then very significant. After the reemission, more and more F* radicals stick to the bottom of the structure. Furthermore, exothermic reactions between the fluorine and silicon provides the surface with energy, which reduces the probability of forming a new passivation layer at the bottom of the structures. This gives rise to self-assembly of vertical nanowire arrays. The schematic diagram of the self-assembled nanowire arrays on the uneven surface is shown in Fig. 1(c).

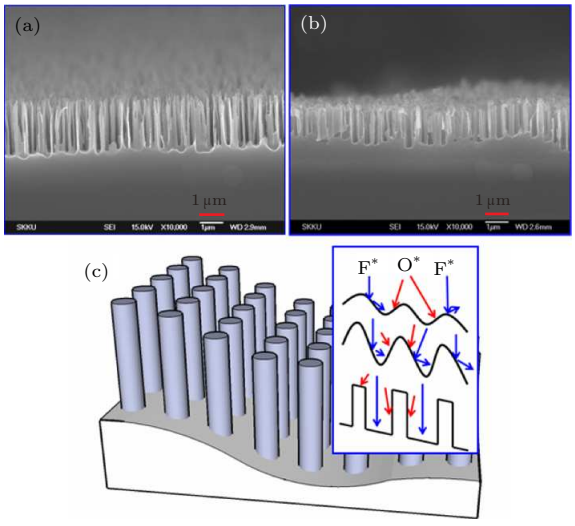

Fig. 1. SEM cross-section images [(a) and (b)] of SiNW arrays on even and uneven surfaces. (c) Schematic diagram of the nanowire arrays on the uneven surface. The inset in (c) shows the schematic diagram of the self-assembled mechanism.

The large-area highly oriented vertical polycrystalline SiNW arrays are formed by plasma etching poly-Si (3 Ω·cm) substrates to fabricate the nanowire solar cells. The plasma etching was performed without using a metal catalyst. The morphology of the SiNWs was controlled by adjusting the etching conditions. For example, SiNW arrays with an average diameter of about 300 nm and an average height of about 1.5 μm could be formed by plasma etching at 600 W of rf source power, 30 W of rf-bias power, 45/45 sccm of SF_6/O_2 gas, 30 mTorr of the pressure for 100 s. The SiNW arrays were then n-doped by spin-coating of a phosphorus (P-509) solution, followed by activation annealing at 900℃ for 30 s. The junction depth of n-polysilicon, x_J, was designed to be about 100 nm with a doping concentration of about 10^{20} cm^{-3}. Subsequently, a 75-nm-thick ITO (on the planar surface) was sputter deposited. The thickness of the wire-array sidewall ITO layer is actually about 30 nm, which is less than 75 nm. The SEM cross-section image and the schematic of the designed ITO-coated radial SiNW p-n junction are shown in Figs. 2(a) and 2(b). Silver (Ag) finger electrodes and an Al electrode were then deposited on the front and back surfaces, respectively, as shown in Fig. 2(c).

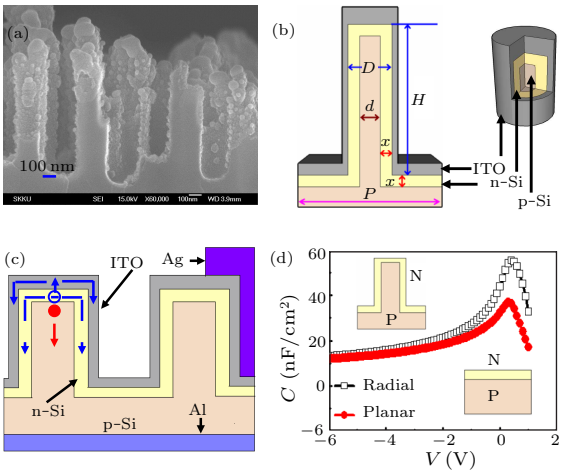

Fig. 2. (a) SEM cross-section image of the ITO-coated SiNW structure. (b) Schematic of the ITO-coated radial SiNW p-n junction structure. (c) Schematic of the fabricated ITO-coated SiNW solar cell. (d) C-V measurement of the radial and planar cells.

The radial doping profiles of the SiNW solar cells are characterized using the capacitance-voltage ($C-V$) method,[2,13] as shown in Fig. 2(d). It is found that the maximum capacitance $C_{\max}$ of the SiNW solar cells (about 55 nF/cm^2) is larger than that (about 35 nF/cm^2) of the planar cells. As the ratio of $C_{\max}$ is proportional to the ratio of the p-n junction areas of the SiNW and the as-cut planar samples,[2] it is understood that the junction area of the SiNW solar cells is about 1.57 times that of the as-cut planar samples. This result is in agreement with the calculated value when the capacitive enhancement factor[2]

$k_C(1.57) = A_{\rm SiNW}/A_{\rm ref} = [P^2 + \pi(D - 2x_J)H]/P^2$, where $A_{\rm SiNW}$ and $A_{\rm planar}$ are the junction areas of the SiNW and planar solar cells, and the diameter D, height H, periodicity P and junction depth x_J of SiNW p-n junctions are set to be 300 nm, 1 μm, 700 nm and 105 nm. The radial p-n junction is formed.

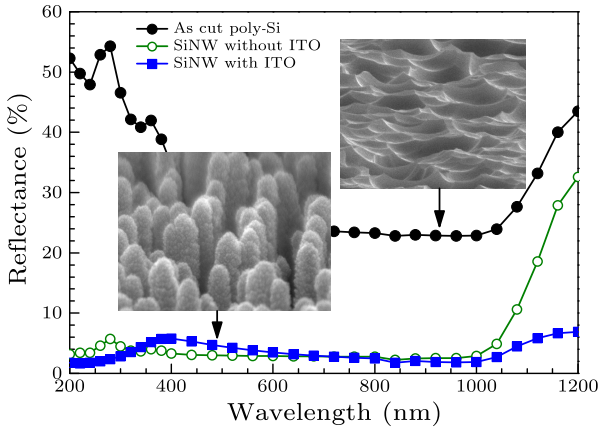

Fig. 3. Reflectance of the different structures: as-cut poly-Si surface, poly-SiNW solar cells without and with ITO coating.

Figure 3 shows the surface light reflectance of various surfaces. The SiNW array structure shows a lower average reflectance (about 2.5%) compared to the as-cut polycrystalline Si surface (about 28%) over the 200–1000 nm wavelength range. This is consistent with the simulation results obtained using the transfer matrix method in Refs. [3,4]. It is understood that the suppressed light reflection is due to the nanowire array. For example, the SiNW with an ITO coating retained the low reflectance (about 2.5%).

Figure 4 shows the current-voltage J–V characteristics of various solar cells obtained at a light illumination intensity of 100 mW/cm^2. The roles of the ITO layer are interpreted with the help of the key parameters listed in Table 1. Firstly, the surface reflectance of the ITO-coated SiNWs is not increased compared to the SiNW cell without ITO coating, as shown in Fig. 3. Secondly, the electrode area ratio of the ITO-coated SiNW solar cells (100%) is much larger than that of the SiNW solar cels without the ITO coating. When the ITO covers the entire surface of the SiNW, although the resistivity of ITO (5×10^{-3} Ω·cm) is larger than that of Ag films (10^{-5} Ω·cm), the generated carriers are readily collected via the shortest path between the p-n junction and the ITO layer and effectively transported to the Ag finger electrode via ITO without recombination, so as to enhance the collection efficiency, as shown by the solid lines in Fig. 2(c). In contrast, the generated carriers can only be collected to the Ag electrode after long-distance diffusion in the n-type substrate of the SiNW solar cells without the ITO coating, as shown by the dashed lines in Fig. 2(c). As a result, the short circuit current density and the fill factor of the ITO-coated SiNW solar cells are obviously increased, compared to the SiNW solar cells without the ITO coating. This causes the conversion efficiency of the ITO-coated SiNW solar cell to be enhanced by about 3 times to 10.1%.

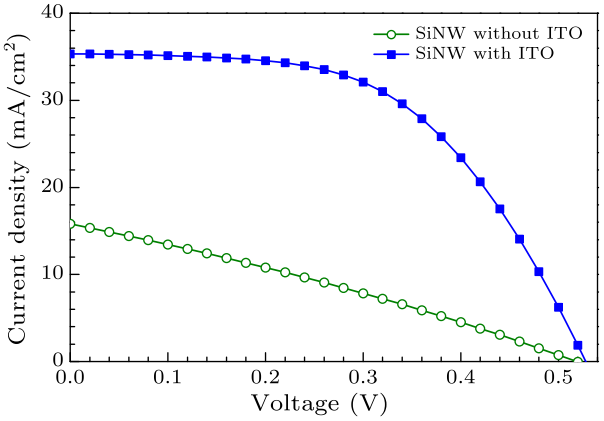

Fig. 4. Current-voltage characteristics of various solar cells under light illumination with an intensity of 100 mW/cm^2.

Note that the ITO layer is designed as a sub-electrode to effectively collect the carriers for the ITO-coated SiNW solar cells. Other transparent conducting materials can also be used in such a self-assembled structure to increase the efficiency of the nanowire solar cells. Optimized materials and deposition methods will be the next steps towards further performance enhancement.

Table 1. The key parameters of the fabricated samples.

Sample	Average reflectance (%)	Electrode area ratio (%)	$J_{\rm SC}$ (mA/cm^2)	Fill factor (%)	Efficiency (%)
SiNW Cell w/o ITO	∼ 2.5	∼ 15 (Ag)	15.2	30	2.4
SiNW Cell with ITO	∼ 2.5	∼ 100	35.4	54.3	10.1

In conclusion, self-assembled nanowire arrays made using plasma etching can be fully coated by ITO to increase the performance of the nanowire solar cells. The self-assembly mechanism is discussed and believed to be the same on both even and uneven surfaces. ITO-coated radial p-n junction poly-crystalline SiNW solar cells are then designed, fabricated and characterized. The ITO-coated SiNW solar cell effectively enhances light absorption and carrier collection, showing enhanced performance via experiments.

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