

# Steep Slope Transistors: Tunnel FETs and Beyond

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**Abstract**—Low voltage transistors are being developed to achieve steep, less than 60 mV/decade, subthreshold swings at room temperature. This paper outlines progress, technical challenges, and applications for these devices.

**Keywords**—NCFET; negative capacitance FET; metal-insulator transition FET; steep transistor, subthreshold swing, TFET; tunnel field-effect transistor

## I. INTRODUCTION

To lower power and increase transistor density in VLSI logic technology, supply voltage must be reduced. This requires that subthreshold swing reduction below 60 mV/decade, the limit of bipolar and field-effect transistors (FETs). Transistors with sub-60-mV/decade slope are called steep transistors. Tunnel field-effect transistors (TFETs) [1, 2] are one of several steep transistors being developed worldwide to outperform the MOSFET at supply voltages less than 0.4 V [3]. Benchmarking of these and other beyond-CMOS transistors for logic vs. 14 nm node CMOS has placed the TFET as the current leading option [4]. However there are other approaches to enable steep slope devices using e.g. ferroelectric gates [5] and complex oxides [6] integrated in conventional transistors. Both of these mechanisms can be applied to the TFET to lower subthreshold swing still further.

## II. TUNNEL FETS

A key figure of merit for steep transistors is the current at which the subthreshold swing is 60 mV/decade,  $I_{60}$  [7]. For a logic transistor to benefit from the steep slope, the low subthreshold swing should be achieved over more than 4-5 decades, with an  $I_{60}$  between 1 – 10  $\mu\text{A}/\mu\text{m}$ . Experimental demonstrations for this key metric are illustrated for the TFET in Fig. 1, which shows measured subthreshold swings as a function of current per unit width. While experiments do not yet meet the desired  $I_{60}$ , simulations show that the channel materials have this capability [8]. Today, technology development is focused on realization of subnanometer equivalent-oxide-thickness gate stacks with low defect densities and low leakage currents, achievement of abrupt, degenerate  $p-n$  junctions with low defect densities, and realization of low contact resistance. While this is a significant list of engineering challenges none are clearly fundamental and each should be solved with continuous effort. The results will reveal the ultimate achievable TFET

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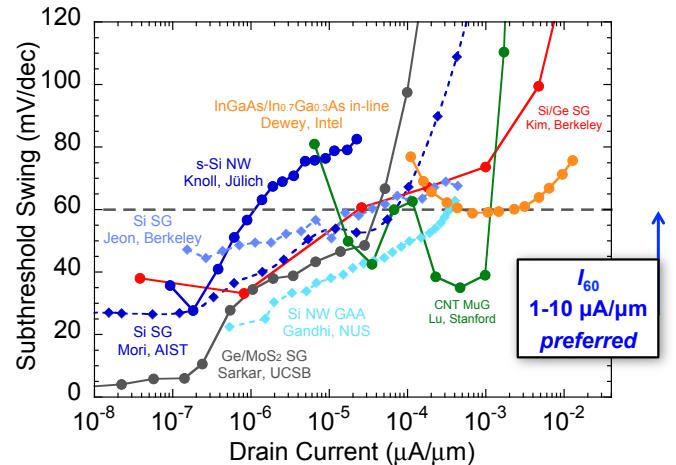


Fig. 1. Selected best TFET experimental reports of subthreshold swing vs. drain current also indicating the desired current  $I_{60}$  for logic applications. These works are cited alphabetically as references [9,10,11,12,13,14,15,16].

performance and the fundamental and practical limits at low voltages.

Two-dimensional, atomically thin channels are of particular interest for TFETs [17,18,19,20]. Sarkar [16] has recently reported the first demonstration of a TFET with subthermal swing using a 2D channel. In this demonstration, the source is p-Ge source, the channel is MoS<sub>2</sub>, and an electrolytic polymer, PEO:LiClO<sub>4</sub> is used to gate the transistor. The measured steep swings are shown in Fig. 1 in comparison with prior reports. To raise the on-current and  $I_{60}$  to levels of interest for VLSI development, many groups are refining methods for contact formation [21,22,23,24],  $p-n$  junction formation [25,26], and atomic layer deposition (ALD) gate stacks [27,28,29]. This technology development for the TFET is a small subset of what is happening in TFETs worldwide, and is representative of TFET technology being refined for use with group IV, III-V, and III-N channel.

## III. STEEP TRANSISTORS BEYOND TUNNELING

Other mechanisms for realization of steep swing transistors are being actively pursued including the use of ferroelectric gates in negative capacitance FETs [5,30,31,32,33,34]. The metal insulator transition (MIT) in complex oxide materials can be utilized in switches if practical methods for electrical triggering can be developed. As an example, subthermal swings have been demonstrated

by incorporating the MIT material into the source of a FET [35].

#### IV. BEYOND DIGITAL APPLICATIONS

SPICE and Verilog models have been developed for steep transistors [36,37,38,39] to enable circuit exploration [40]. In addition to digital applications [41], steep devices are also being evaluated for analog circuit applications [42] to lower power and improve the efficiency of RF circuits and systems. The steep transistor should naturally find application in energy harvesting as a zero bias rectifier.

#### V. CONCLUDING REMARKS

The materials options for steep transistors has continued to expand. Each channel material requires its own gate stack, junctions, and contact technology. As a result there are many laboratories working on TFETs in a wide range of materials and exploring a similiar wide range of transistor geometries. Because there are many materials with potential to outperform CMOS at low voltage a down selection to a preferred channel material and geometry has not been made. Will the steep transistor be part of the front-end or back-end of the process? This is part of the discussion.

One can anticipate that the first steep transistors with measured performance beyond the capabilities of CMOS will coalesce the community and technology will advance more quickly. Process technologies with potential to transition into foundries or start-ups will make the earliest impact. Successful development of steep transistors will provide circuit designers with a low-voltage transistor that will revolutionize ultralow power systems.

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