Excitation/Inhibition Balancing in 2D Synaptic Transistors With Minority-Carrier Charge Dynamics

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***Abstract*— Most of the reported synaptic FETs with majority-carrier charge traps suffered from unbalanced excitatory and inhibitory behaviors. Here, we demonstrate an ambipolar WSe_2 synaptic FET with the charge dynamics of both electron and hole charge traps. The device shows balanced excitation and inhibition to a gate stimulation, due to the participation of minority-carrier charge traps. As a result, a nearly zero asymmetry with low nonlinearity of 0.04 is realized in long-term potentiation and depression (LTP/LTD). Good device repeatability is confirmed by device-to-device and cycle-to-cycle tests. A high accuracy of 92.8% is realized in the pattern recognition simulation. The proposed devices possess great potential in high-accuracy neuromorphic computing applications.**

***Index Terms*— Synaptic transistor, charge dynamics, neural plasticity.**

I. Introduction

RECENTLY, neuromorphic computing that emulates the nervous system of the human brain with artificial neural networks is developing rapidly [1]. Two-dimensional (2D) field-effect transistors (FETs) with resistance-switching functions have been investigated as artificial synapses. Distinct physical mechanisms causing resistance switching have been reported, including charge dynamics [2], [3], floating gate [4], ferroelectric polarization [5], [6], [7], [8], and ion migration [9]. Among them, charge-related synaptic behaviors are of great interest due to their easy accessibility. Charge traps can be induced by simple surface modification in regular FETs. Complex fabrication processes required to realize heterostructures of the floating gate and ferroelectric devices are avoided.

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Balanced excitatory/inhibitory characteristics are essential for robust neuronal selectivity. However, they have rarely been achieved in previously reported charge-related synaptic FETs with only majority-carrier charge traps. Excitatory and inhibition behaviors of charge dynamics-based synaptic FETs are greatly correlated to the charge trapping and release rates. Their different time scales lead to a significant discrepancy in conductance change under excitatory and inhibitory stimulations. As a result, much weaker inhibitory behaviors than excitatory behaviors are usually observed [10], [11], [12], [13], therefore limiting neuronal selectivity and hindering neuromorphic computing application.

Here, we demonstrated the 2D ambipolar synaptic FETs with charge dynamics of both majority and minority carriers exhibiting balanced excitatory/inhibitory behaviors. An excellent nonlinearity approaching 0.04 and a nearly ideal asymmetry value of 0 were achieved in the LTP/LTD under incremental pulse stimulations. Cycle-to-cycle and device-to-device tests suggest good device repeatability. Digit recognition was simulated and a high recognition accuracy of 92.8% is achieved. The proposed device shows great potential for high-accuracy neuromorphic computing.

II. Experimental Details

Fabrication of the WSe_2 FETs started from mechanical exfoliation of few-layer WSe_2 flakes (6∼8 nm) onto a Si substrate capped with 300 nm SiO_2. Relatively thick flakes are used to avoid significant device performance variations induced by bandgap differences or substrate effects. A 5 nm/50 nm In/Au stack was evaporated as electric contacts. As-fabricated WSe_2 FETs were treated in diluted hydrogen peroxide solution (H_2O_2, 35%wt in H_2O) for 200 s, then washed with deionized water and dried with nitrogen.

Room-temperature electrical measurements were performed in a vacuum probe station at 0.1 Pa using a circuit sketched in Fig. 1(a). The highly p-doped Si substrate ($<0.005\ \Omega \cdot$cm) was employed as a back gate electrode. The presynaptic spike was mimicked by applying the gate voltage (V_G) pulse, while the channel current (I_D) at a constant drain voltage (V_{DS}) of 0.5 V was regarded as the postsynaptic current (PSC).

III. Results and Discussion

The schematic and optical microscope images of the treated WSe_2 FET are shown in Fig. 1(a) and Fig. 1(b), respectively. H_2O_2treatment partially oxidizes the WSe_2 surface, resulting in Se vacancies (Se^{2+}) and radical adsorption (OH^-, O_2^-) as

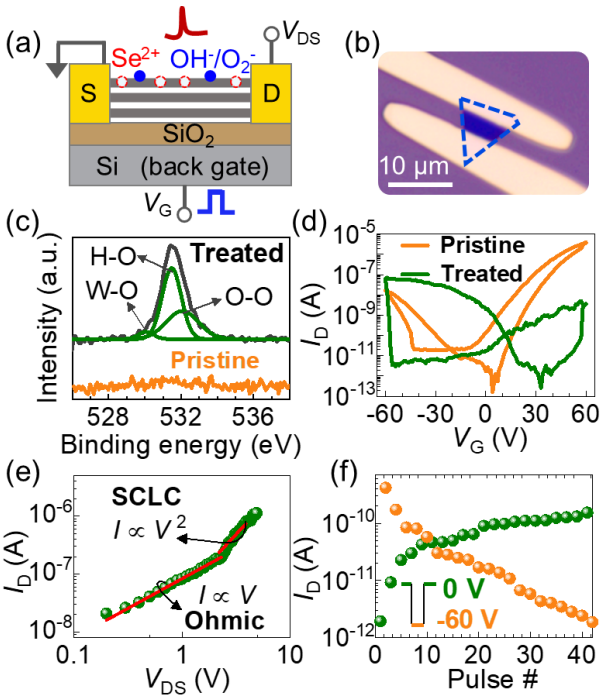

Fig. 1. (a) Schematic and (b) optical microscope image of a WSe_2 synaptic FET. (c) O 1s XPS spectra of pristine and treated WSe_2. (d) Transfer curves of the WSe_2 FET. (e) Output curve measured at $V_G = 60$ V. (f) Current response to a 500 ms gate pulse train of −60 V/0 V.

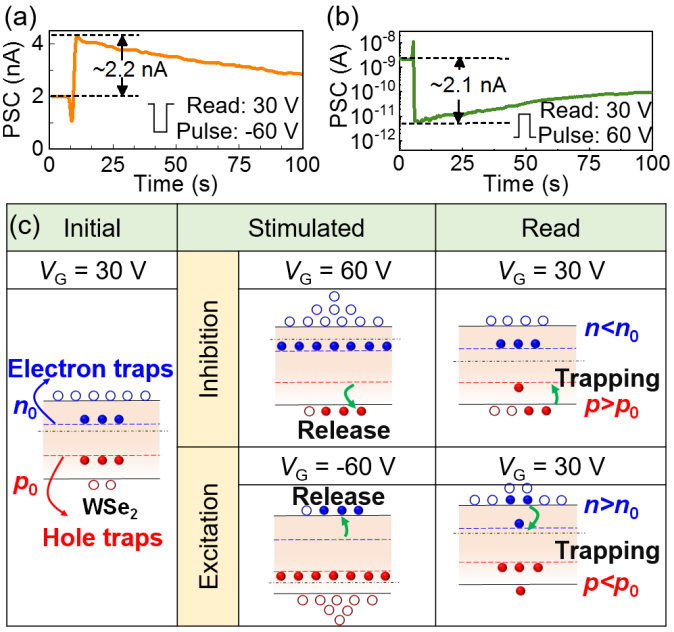

Fig. 2. (a) Excitatory and (b) inhibitory PSC under 300 ms negative and positive gate pulses, respectively. (c) Band diagrams showing the mechanisms of inhibitory and excitatory processes.

electron and hole traps, respectively [14], [15]. This can be experimentally verified using x-ray photoelectron spectroscopy (XPS). A reduced Se/W ratio from 2.03 to 1.97 after treatment indicates the formation of 3% Se vacancies. An obvious O1s signal is noticed after the treatment (Fig. 1(c)). The peaks at 531.47 eV and 532.06 eV correspond to O-H and O-O bonds, respectively [16], implying surface adsorptions of OH^- and O_2^-. Se^{2+} and oxidative absorptions create defect levels near the conduction band and valence band, respectively, as calculated by density functional theory [17].

The existence of charge traps leads to hysteresis behaviors in WSe_2 FETs. Fig. 1(d) plots the transfer curves measured before and after H_2O_2 treatment. The pristine device shows n-dominated ambipolar characteristics with a weak hysteresis. After the treatment, significantly enhanced hysteresis is noted in both electron and hole branches. At low V_{DS}, ohmic conduction is indicated by a linear I-V correlation, as shown in Fig. 1(e). Shallow trap space charge limited conduction (SCLC) behavior, *i.e.* the I-V correlation known as $I_D \propto V_{DS}^{\alpha} (\alpha = 1.5 \sim 2)$, is observed at high V_{DS}, suggesting the presence of shallow charge traps [18]. Noted, a high gate voltage of 60 V is necessary to reduce the contact resistance and facilitate the channel-dominated transport, as the SCLC regime cannot be observed with considerable contact resistance. The co-existence of electron and hole charge traps can also be verified by measuring I_D response to a gate pulse train of −60 V/0 V (500 ms) as plotted in Fig. 1(f). With the increased number of pulses, I_D read at $V_G = -60$ V, where the hole dominates, keeps decreasing due to the trapping of holes. On contrary, I_D read at $V_G = 0$ V (read right after the −60 V gate pulse is retracted) with electron-dominated conduction increases due to the release of electrons.

The dual-carrier charge traps-involved charge dynamics can emulate both excitatory and inhibitory behaviors. Figs. 2(a) and 2(b) show the typical excitatory PSC and inhibitory PSC in response to the negative and positive gate pulses (300 ms), respectively. Read is performed at $V_G = 30$ V to set electrons as the majority carriers. The balanced excitatory and inhibitory behaviors that last more than 100 s are achieved with the same PSC change of ∼2 nA.

Fig. 2(c) explains the mechanisms of the excitation and inhibition balancing assisted by the minority-carriers trapping process. At $V_G = 30$ V, WSe_2 is electron dominated, while part of electron/hole charge traps is occupied. A negative pulse of −60 V pushes the Fermi level towards the valence band, which releases electrons and traps holes. Since re-trapping is a slow process, the released electrons can last for a relatively long period [19]. The effective electron density is, therefore, enhanced, resulting in excitatory behavior in the electron-dominated FET. When a positive pulse of 60 V is applied, the Fermi level is pushed upwards, provoking electron trapping and the release of holes. The resulting increment of hole density causes the reduction of effective electron density under the thermal equilibrium compared to the initial state. Consequently, the inhibitory behavior emerges.

On contrary, in a device with only majority-carrier (electron) traps, the trapped electrons are instantaneously released once the positive pulse is retracted. Consequently, the inhibition decays rapidly, and therefore, is not measurable. To verify that, an additional Ti-contacted WSe_2 FET was fabricated for comparison. Unipolar transfer characteristic is therefore measured, as the Fermi level is pinned near the conduction band minimum at the Ti-WSe_2 contact interface (Fig. 3(a)) [20]. Furthermore, hole conduction and hole trap-related charge dynamics are strongly suppressed. Subsequently, nearly no inhibitory behavior can be observed (Fig. 3(b)).

LTP and LTD are the basis for learning and memory formation. Fig. 4(a) plots the LTP and LTD responses of

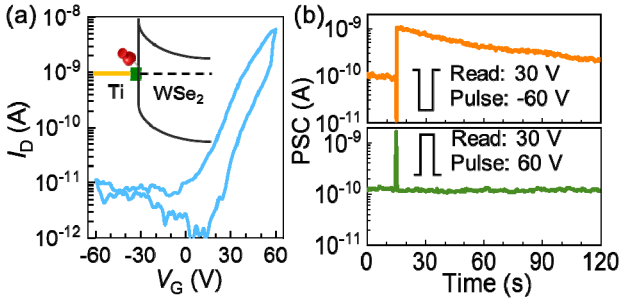

Fig. 3. (a) Transfer curve of a Ti-contacted unipolar WSe_2 FET after surface treatment. (b) Exhibitory and inhibitory behaviors under 300 ms gate pulses.

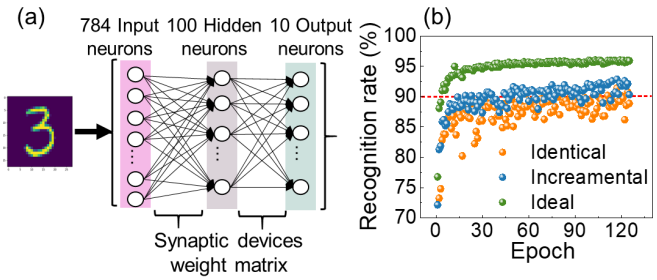

Fig. 5. (a) The schematic of the neural networks. (b) The recognition accuracy of the synaptic FET under identical and incremental pulse schemes.

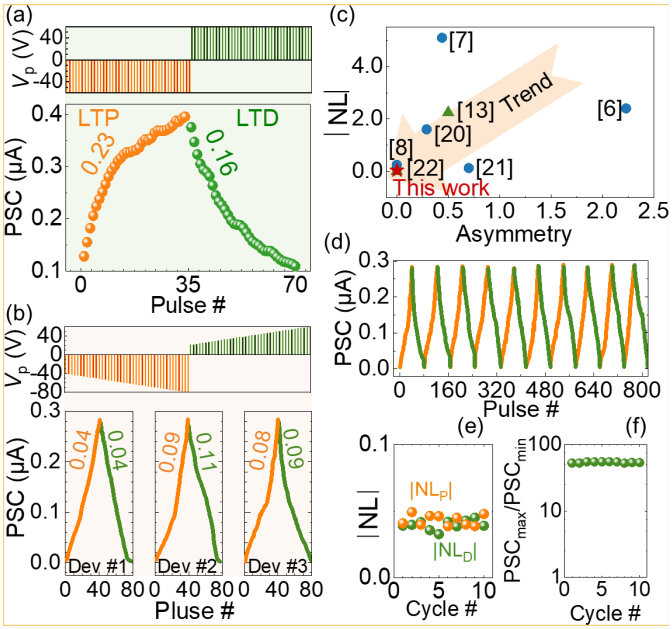

Fig. 4. LTP and LTD characteristics measured under (a) identical pulse scheme and (b) incremental pulse scheme in three independent WSe_2 synaptic FETs. (c) Benchmarking of $|NL|$ and asymmetry extracted from device #1 with previously reported synaptic devices. (d) Cycle-to-cycle test with device #1 using incremental pulse stimulations. (e) Nonlinearity values and (f) PSC_{max}/PSC_{min} ratio extracted in different operation cycles. All read is set at 30 V.

a FET subjected to 70 identical pulse stimulations. Low nonlinearity values of $|NL_P| = 0.23$ and $|NL_D| = 0.16$ are extracted [21]. Generally, the LTD process in devices with weak inhibition is dominated by the decay of the excitation current, showing unsatisfactory nonlinearity. The contribution from strengthened inhibition to the LTD process enhances the efficiency of gate pulse modulation and reduces the nonlinearity. Thanks to the balanced excitation and inhabitation, a low asymmetry value calculated as $|NL_P| - |NL_D| = 0.07$ is obtained. The PSC_{max}/PSC_{min} ratio reaches a high value of $\sim 40\times$.

The linearity and symmetry can be further optimized by employing the incremental pulse scheme. Fig. 4(b) plots the PSC response under the stimulations of 80 incremental negative and positive pulses (LTP: -41 V to -80 V, 1 V steps; LTD: 21 V to 60 V, 1 V step). PSC_{max}/PSC_{min} ratio is further improved to >50, which is desired for high neural network accuracy. Extremely low nonlinearity $|NL_P| \approx |NL_D| = 0.04$ and nearly zero asymmetry values are achieved. Fig. 4(c) plots the benchmarking of the extracted $|NL|$ and asymmetry in comparison with previously reported synaptic FETs [22], [23]. $|NL|$ and symmetry of LTP/LTD of our FET are far better than the previously reported charge-related synaptic FETs and almost on par with ferroelectric FETs.

The device's repeatability is then discussed. Identical LTP/LTD characteristics are measured in three FETs (Fig. 4(b)). Similar $|NL_P|$ and $|NL_D|$ values within the same order of magnitude highlight good device-to-device repeatability. Moreover, LTP/LTD behaviors are well maintained in terms of $|NL|$ and symmetricity in 10 operation cycles with device #1 as shown in Fig. 4(d). Fittings suggest a low mean $|NL|$ value of 0.04 and a variation within 10% among different cycles (Fig. 4(e)). The PSC_{max}/PSC_{min} ratio maintains a consistent value of $\sim$53.8 with a 2% variation (Fig. 4(f)).

To investigate the potential of our WSe_2 synaptic in pattern recognition, a two-layer multilayer perceptron neural network is developed based on the measured LTP and LTD data of device #1 to simulate the learning number from the MNIST handwritten digits (28×28 pixels Fig. 5(a)). The network consists of 784 input layer neurons, 100 hidden layer neurons, and 10 output layer neurons. After 125 epochs, the maximum recognition accuracy reaches 90% with identical pulses and it is further enhanced to 92.8% with incremental pulses on account of improved linearity and symmetry in synaptic weight change (Fig. 5(b)). This value is close to that of 95% of an ideal device for the software baseline. Further improvement is expected with increased hidden layer neurons and training epochs.

IV. Conclusion

In conclusion, balanced excitatory/inhibitory behaviors have been realized in 2D WSe_2 synaptic FETs owing to the coexistence of electron and hole charge dynamics. The linear and symmetric LTP/LTD are shown with incremental pulse stimulations. Good device repeatability is proved by device-to-device and cycle-to-cycle tests. Our proposed device achieves a recognition accuracy rate as high as 92.8% when performing the recognition tasks. This research demonstrated a promising strategy for using simple charge-related FETs for high-performance neuromorphic devices.

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