Deep level transient spectroscopy on charge traps in high-k ZrO$_2$

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ARTICLE INFO

ABSTRACT

The deep trap properties of high-dielectric-constant (k) ZrO$_2$ thin films were examined by deep level transient spectroscopy (DLTS). The hole traps of a ZrO$_2$ dielectric deposited by sputtering were investigated in a MOS structure over the temperature range, 375 K–525 K. The potential depth, cross section and concentration of hole traps were estimated to be $\sim$2.5 eV, $\sim$1.8$\times$10^{-16} cm^2 and $\sim$1.0$\times$10^{16} cm^{-3}, respectively. DLTS of ZrO$_2$ dielectrics can be used to examine the threshold voltage shift (ΔV_{th}) during the operation of SONOS-type flash memory devices, which employ high-k materials.

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1. Introduction

High-dielectric-constant (k) dielectrics have been investigated extensively for solid-state and nanowire-based device applications [1,2]. Along with other high-k dielectrics, e.g., Al$_2$O$_3$ [3], Ta$_2$O$_5$ [4–6], HfO$_2$ [7,8], La$_2$O$_3$ [7,8] etc., ZrO$_2$ is considered to be a potential replacement for SiO$_2$ gate dielectrics in nanoscale semiconductor device owing to its high-k value ($\sim$25) and large band gap ($\sim$5.8 eV) [1,9]. Its properties, e.g. electrical performance [10–12], thermody-namic stability [13], interface quality [13,14], and gate material compatibility [15] etc., have been studied extensively. However, as a critical factor for the reliability of future memory devices, the properties of the traps or electrically active defects in high-k materials are not completely understood. Deep level transient spectroscopy (DLTS) is used widely compared to other techniques for examining the trap properties, such as Rutherford backscattering spectroscopy, charge pumping, and low-temperature capacitance transient method etc. [16–19], because of its ability to identify the majority/minority traps, superior accuracy and general applicability to both bulk and interfacial trap investigations in p–n junctions, Schottky junctions [20], metal–oxide–semiconductor (MOS) capacitor [21], and even oxide–nitride–oxide (ONO) structures [22]. In this study, the trap properties of a ZrO$_2$ thin film on p-type Si substrate were examined by DLTS. It was estimated that hole traps in ZrO$_2$ have a potential depth of $\sim$2.5 eV from its valence band edge, a cross section of $\sim$1.8$\times$10^{-16} cm^2, and a concentration of $\sim$1.0$\times$10^{16} cm^{-3}. These results are consistent with previous works [23,24]. Theoretically, this method is also applicable to other high-k dielectric films.

2. Experiment

To examine the hole trap properties, p-type silicon was used as a substrate with a native oxide as the buffer layer. 10-nm-thick ZrO$_2$ was deposited on unheated substrates using a Zr target at a power of 300 W and pressure of 15 mTorr with 20 sccm Ar and 20 sccm O$_2$. A 150-nm-thick Au layer was deposited as a gate electrode by thermal evaporation with a Ti buffer layer. The diameter of the gate pattern formed by the shadow mask was 1 mm. The reference MOS capacitor with a 10-nm-thick SiO$_2$ dielectric was prepared to compare with the DLTS spectra of the ZrO$_2$ capacitor. The experimental setup for the DLTS was configured using a pulse generator (Agilent 81110A), a precision LCR meter (Agilent E4980A), and a temperature controller. The capacitance transient after a 0.19 s pulse was monitored over the temperature range, 375 K–525 K.

3. Theory

Fig. 1(a) shows the energy band of the MOS capacitor with the ZrO$_2$ dielectric [1]. During the DLTS measurement, a small quiescent bias V_a is needed to keep the substrates under depletion or weak inversion in order to prevent disturbances of the minority carriers in the inversion layer, which can induce the charging and discharging of minority traps at the interface and DLTS signals, as shown in Fig. 1(b). A small V_a was used to suppress the effect of electric field on the carrier emission rates [25]. Before the majority carrier pulse V_b was added ($t < t_o - 0.19$ s), V_a was applied to maintain the deep traps in the discharged state, as shown in Fig. 1(c-i). Subsequently, V_b (-4 V) was applied ($t_o - 0.19$ s $< t < t_o$) to drive the substrate into accumulation. Both the dielectric and substrate deep traps near the interface shift over the Fermi level (φ_f) and capture the free carriers (holes in this work) that accumulate at the interface, as shown in Fig. 1(c-ii). After V_b ($t > t_o$), the deep traps are restored to their initial potential, and

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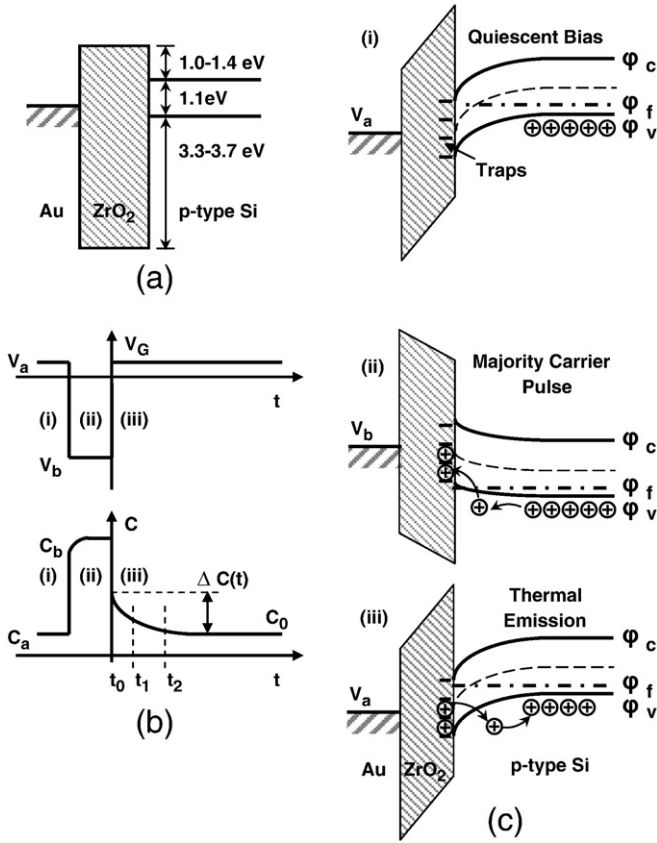E-mail address: yoowj@skku.edu (W.J. Yoo).

Fig. 1. Schematic diagram of the DLTS technique in n-MOS structure. (a) Energy band of the MOS capacitor with the ZrO$_2$ dielectric. (b) Voltage–time (V–t) and corresponding capacitance–time (C–t) diagrams indicating the majority carrier pulse V$_b$ and capacitance transient, respectively. (c) Energy band diagrams before (i), during (ii) and after (iii) the majority carrier pulse.

temperature-dependent discharging of the trapped carriers causes a capacitance transient [20], as shown in Fig. 1(c-iii).

4. Results and discussion

Capacitance–voltage (C–V) measurements for both ZrO$_2$ and SiO$_2$ capacitors were performed before DLTS to verify their electrical behavior and determine the optimum bias conditions for DLTS application, as shown in Fig. 2. For a SiO$_2$ capacitor, negligible capacitance hysteresis was observed when a forward/reverse (F/R) scan was performed, since the deep trap density is negligibly low in
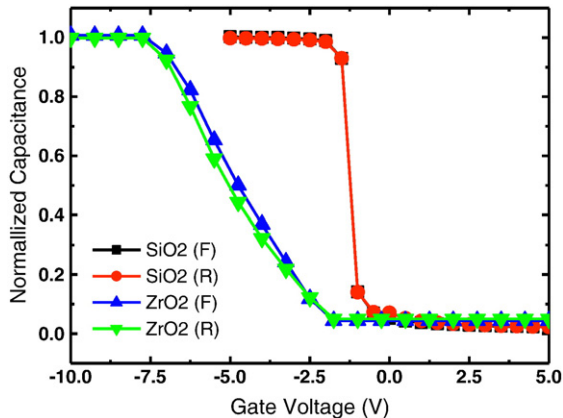
high-quality thermal SiO$_2$ [1]. On the other hand, hysteresis was clearly observed in the ZrO$_2$ device, indicating the existence of high-density deep traps. Free carriers can be captured by these traps during the F/R scan, giving rise to a memory window, ΔV, of ~0.5 V.

The DLTS signal obtained from the ZrO$_2$ capacitor may respond to the traps in the Si substrate, SiO$_2$ buffer layer or ZrO$_2$ dielectric. Therefore, a SiO$_2$ capacitor, where the DLTS signal only responds to the traps in the Si substrate or SiO$_2$ dielectric, was utilized as a reference for comparison. It is reasonable to assume that the DLTS spectra for the traps in the substrate and buffer layer are identical in both ZrO$_2$ and SiO$_2$ capacitors because identical substrates and SiO$_2$ dielectrics with the same properties were used. Therefore, the differences in the DLTS spectra were due only to the different dielectric deep traps. According to the experimental results, the DLTS spectra of the ZrO$_2$ capacitor was observed at a higher temperature (approximately 480 K) than that of the SiO$_2$ capacitor (approximately 380 K), indicating that the ZrO$_2$ dielectric is the origin of the observed traps, as shown in Fig. 3(a). Various thermal emission rates $e_n(T)$ can be obtained as $e_n(T) = \ln(t_2/t_1)/(t_2 - t_1)$ [20], where T is the absolute temperature, t_1 and t_2 are the selected scanning periods ($t_2 - t_o > t_1 - t_o$). In order to obtain accurate data, DLTS measurements were applied under various pulse levels ($V_b = 0.1$ V, 0.3 V, 0.5 V and 0.7 V) and rate windows ($t_1/t_2 = 1/2$, 1/3 and 1/5). Fig. 3(b) shows the corresponding Arrhenius plots for the ZrO$_2$ sample from the following equation [16],

$$\ln \frac{e_n(T)}{T^2} = -\frac{\Delta E_{trap}}{k_B} \cdot \frac{1}{T} + \ln \frac{4\sqrt{6}k_B^2\pi^{3/2}m^*}{h^3}\sigma \qquad (1)$$
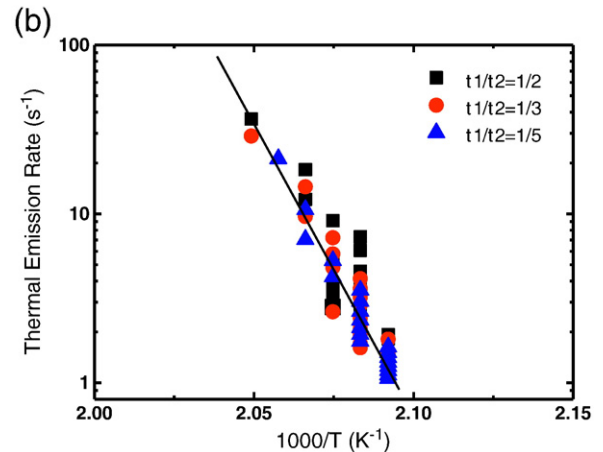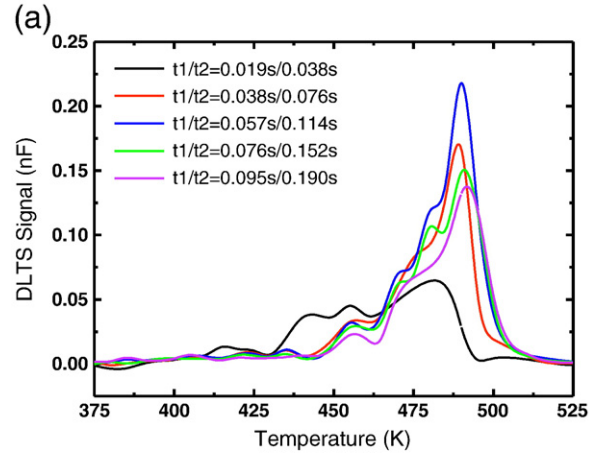

Fig. 2. C–V characteristics of the n-MOS capacitors with the SiO$_2$ and ZrO$_2$ dielectrics at room temperature (300 K).

Fig. 3. (a) DLTS spectra and (b) corresponding Arrhenius plots of the ZrO$_2$ capacitor when $V_b = 0.5$ V.

where k_B is Boltzmann's constant, h is Planck's constant, m^* is the effective carrier mass ($0.56 m_o$ in this work),[26] ΔE_{trap} is the trap depth and σ is the cross section. Since Eq. (1) is a linear function of $1/T$, ΔE_{trap} and σ can be obtained by linear regression from the slope and constant, respectively. For example, the slope for the SiO_2 sample suggests that $\Delta E_{\text{trap}} \approx 0.3$ eV. For the ZrO_2 sample, the average slope (-2.92×10^4 K) indicates $\Delta E_{\text{trap}} = -2.92 \times 10^4$ K $\times$ (-0.0259 eV/ 300 K) ≈ 2.5 eV, while the constant (12.7) gives rise to $\sigma = \exp 12.7 \times$ $(6.63 \times 10^{-34} \text{ J s})^3 / [4 \times 6^{1/2} \times (1.38 \times 10^{-23} \text{ J K}^{-1})^2 \times 3.1415^{3/2} \times$ $0.56 \times 9.1 \times 10^{-31} \text{ kg}] \approx 1.8 \times 10^{-16} \text{ cm}^2$. According to Fig. 1(c), there are high-density deep traps in ZrO_2 located very close to the substrate. As reported previously, the deep traps of ZrO_2 may be induced by an intensive reaction between SiO_2 and ZrO_2 [23,24]. Considerable intermixing is observed at the ZrO_2/SiO_2 interface because ZrO_2 is highly reactive with SiO_2, and the thickness of the interfacial layer is ~2 nm. Therefore, high-density traps may be generated in the interfacial layer. The deep traps (~2.5 eV from the valence band edge of ZrO_2) obtained by DLTS in this study are similar to the reported results (~2.1 eV) [27]. Since high-k material properties are sensitive to their fabrication processes [1,9], this overestimation could be induced by different deposition conditions, treatment processes and observation methods.

In addition, the relative concentration of deep traps in ZrO_2 can be estimated by $N_{\text{trap}}/N_d = 2\Delta C(t)/C_0$ [20,22], as shown in Fig. 4(a), where N_d is the substrate doping concentration ($5 \times 10^{16} \text{ cm}^{-3}$), N_{trap} is the estimated deep trap concentration, $\Delta C(t)$ is the maximum amplitude of the capacitance transient, and C_0 is the quiescent capacitance. In this study, the average $\Delta C(t)$ and C_0 values were ~$2.0 \times 10^{-6} \text{ F cm}^{-2}$ and ~$2.2 \times 10^{-5} \text{ F cm}^{-2}$, respectively. Therefore,

N_{trap} was estimated to be $N_{\text{trap}} = 2 \times 2.0 \times 10^{-6} \text{ F cm}^{-2} \times 5 \times 10^{16} \text{ cm}^{-3}/$ $(2.2 \times 10^{-5} \text{ F cm}^{-2}) \approx 1.0 \times 10^{16} \text{ cm}^{-3}$. Fig. 4(b) shows the temperature dependence of C_0, where the abrupt increase in the range of 450 K– 475 K is due to the prompt discharging of the traps. Both the trap concentration and quiescent capacitance observed by the small V_b (0.1 V and 0.3 V) are obviously different to those observed by the large V_b (0.5 V and 0.7 V). These may be due to the non-uniform spatial distribution of the deep traps.

5. Conclusion

The deep traps of ZrO_2 thin films were investigated using C–V measurements and DLTS. The trap depth, cross section and concentration in ZrO_2 thin films were estimated to be ~2.5 eV, ~$1.8 \times 10^{-16} \text{ cm}^2$ and ~$1.0 \times 10^{16} \text{ cm}^{-3}$, respectively. According to this work, the validity of DLTS to examine the trap property in the high-k dielectric was confirmed. Therefore, it can be a powerful tool for analyzing the trap properties that can cause V_{th} instability in memory devices.

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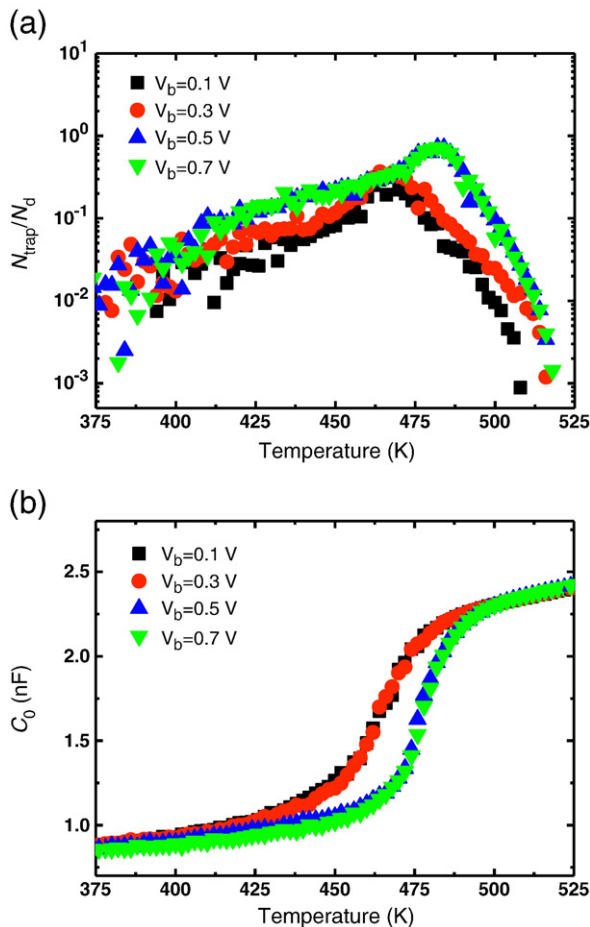

Fig. 4. (a) Relative concentration N_{trap}/N_d and (b) quiescent capacitance C_0 as a function of temperature under different pulse levels V_b.