Second-Bit-Effect-Free Multibit-Cell Flash Memory Using Si$_3$N$_4$/ZrO$_2$ Split Charge Trapping Layer

Gang Zhang, Student Member, IEEE, Seung-Hwan Lee, Chang Ho Ra, Hua-Min Li, and Won Jong Yoo, Senior Member, IEEE

Abstract—In this paper, a Si$_3$N$_4$/ZrO$_2$ split charge trapping layer (SCTL) is proposed for multibit-cell Flash memory. The complementary potential wells of Si$_3$N$_4$/ZrO$_2$ storage nodes enable independent node control when the Fowler–Nordheim (F–N) method is applied for programming/erasing (P/E). Experiment and simulation results suggest that the 2-bit (2-b) charge storage is accomplished by physical data node separation for the SCTL rather than charge injection control. The well-confined charge storages suppress the second-bit effect, enabling excellent 2-b data clearance for short-channel SCTL devices. It was found that the remaining memory windows after $10^5$ s decrease, dependent on the difference of the trap properties between Si$_3$N$_4$ and ZrO$_2$.

Index Terms—Flash memory, second-bit effect, Si$_3$N$_4$/ZrO$_2$, split charge trapping layer (SCTL).

I. INTRODUCTION

RECENTLY, multibit-cell Flash memory based on physically separated charge-storage nodes and forward/reverse data detection (F/R-read) have been investigated extensively [1]–[5] for its great potential in future ultra-high-density data storage application [6]. However, the charge-injection-controlled multi-bit cells are rapidly approaching the scaling limits due to the second-bit effect. For example, the scalability for 2-b cells operated by channel hot electron injection (CHEI) and hot hole injection (HHI) was reported to be 110–170 nm [7]–[10]. A dual-bit high-injection MOS memory with a split Si$_3$N$_4$ trapping layer was proposed to suppress the second-bit effect. However, its scalability (∼150 nm) of the split-gate devices was still limited by the source-side injection (SSI) control [5]. Moreover, the data clearance and array reliability of the 2/4-bit cells are degraded by the second-bit-effect-induced F/R-read disturbances [11].

The second-bit effect is induced by the inefficient screening of the surface potential created by the locally injected charges [11]. For short-channel devices, the spread of charge injection results in inevitable mutual disturbances between the separated storage nodes [11]. However, it is difficult to confine the spread of CHEI/HHI [9]–[11], and the maintenance of 2-b data clearance by optimizing the CHEI/HHI profiles is critical for NROM-type devices [11]. One alternative is to realize the 2-b operation by using the F-N method based on self-initialized node control. If the stored charge is accurately confined by the physical dimension of data nodes, the charge spread can be eliminated, and the second-bit effect is expected to be suppressed.

In this paper, a Si$_3$N$_4$/ZrO$_2$ SCTL is proposed for second-bit-effect-free multi-bit-cell application. Si$_3$N$_4$ has small conduction band ($\Delta\phi_c = 1.1$ eV) and large valence band ($\Delta\phi_v = 2.6$ eV) offsets with respect to SiO$_2$, while ZrO$_2$ has a large $\Delta\phi_c = 2.1$ eV and small $\Delta\phi_v = 1.1$ eV [12]. The complementary band structures of Si$_3$N$_4$/ZrO$_2$ result in reciprocal tunneling properties for electrons and holes when the F-N method is applied for P/E, in that ZrO$_2$ enhances electron tunneling while it suppresses hole tunneling, whereas Si$_3$N$_4$ suppresses electron tunneling while it enhances hole tunneling [9], [13]. The independent control of Si$_3$N$_4$/ZrO$_2$ storage nodes by $\pm V_g$ thus becomes feasible, and the F/R-read enables a 2-b operation [1]–[3]. Experiment and simulation results suggest that charges by physical separation in the SCTL are confined better in the storage nodes, compared with those by charge injection control. With a well-confined charge storage, the second-bit effect is suppressed, and an excellent 2-b data clearance is maintained for short-channel SCTL devices. However, the improvement of data retention still requires further investigation.

II. DEVICE DESIGN AND FABRICATION

The schematic of a device structure is shown in Fig. 1(a), and the complementary potential wells of the Si$_3$N$_4$ and ZrO$_2$ nodes...
are shown in Fig. 1(b). Si$_3$N$_4$ and ZrO$_2$ nodes share the channel length ($L_g$) to enable F/R-read at the same read biases [11], and the block oxide extension prevents the charge from migrating between the separated storage nodes. The process flow of poly-silicon–oxide–nitride–oxide–silicon (SONOS)-type devices with a Si$_3$N$_4$/ZrO$_2$ SCTL is shown in Fig. 2(a). After pre-gate cleaning, an about 3-nm-thick tunnel oxide (SiO$_2$) was thermally grown on a p-type Si substrate. Subsequently, an about 6-nm-thick ZrO$_2$ was deposited by the dc sputtering of Zr target in an Ar+$O_2$ ambient. After post-deposition annealing at 600 °C for 30 s, the first gate patterning was performed by a deep UV optical lithography stepper with a KrF laser source of 248-nm wavelength. After plasma etching, the ZrO$_2$ and the $Zr_xSi_{1-x}O_2$ interfacial layers were removed. About 5.8 nm of Si$_3$N$_4$ was then deposited by plasma-enhanced chemical vapor deposition (PECVD) to cover the formed ZrO$_2$ node and the remaining photoresist (PR). The Si$_3$N$_4$ layer that covers the PR (with a thickness of $\sim$0.3 μm) was removed during PR lift-off, and the split Si$_3$N$_4$/ZrO$_2$ charge trapping layer was formed. About 10 nm of SiO$_2$ was then deposited by low-pressure CVD (LPCVD) to cover the SCTL and fill the gap between the Si$_3$N$_4$/ZrO$_2$ nodes for the block oxide and block oxide extension formation. After an $\sim$150-nm-thick TaN gate electrode formation and the second gate patterning, As$^+$ was implanted with doses of $8 \times 10^{14}$ cm$^{-2}$ and $4 \times 10^{15}$ cm$^{-2}$ and energies of 10 and 35 keV for the shallow source/drain (S/D) extension and deep S/D regions, respectively, followed by activation annealing at 1000 °C for 5 s.

The formation of the gate structure with separated Si$_3$N$_4$/ZrO$_2$ storage nodes was confirmed by the cross-sectional transmission electron microscopy (TEM) image, as shown in the inset of Fig. 2(b). The layer thicknesses were measured by an ellipsometer during the process and confirmed by the TEM image after the device fabrication. The formation of the Si$_3$N$_4$/ZrO$_2$ nodes was proven by energy-dispersive X-ray spectroscopy. Good F/R-read $I_d$–$V_d$ characteristics for a 220-nm fresh device which enables the reliable gate control for the SCTL gate stack are shown in Fig. 2(b). The equivalent oxide thicknesses (EOTs) of the ZrO$_2$ and Si$_3$N$_4$ storage stacks are estimated to be $\sim$13.3 and $\sim$15.9 nm by capacitance–voltage ($C$–$V$) measurements, respectively [14].

It is noticed that the separated storage nodes are misaligned with the gate patterning. This brings about complex fabrication and integration processes for the SCTL devices. However, the
2-b cell scalability of the SCTL devices can still be enhanced, compared with that of the NROM-type 2-b cells if the second-bit effect is suppressed. The advanced lithography technology used in the 15-nm planar memory processing presents a solution for the fabrication of short-channel SCTL devices [15]. In contrast, the scalability of the NROM-type 2-b cells is limited at 110–170 nm due to the second-bit effects, rather than the processing technologies.

III. SCTL CELL P/E PROPERTIES

Based on the complementary potential wells of the Si$_3$N$_4$/ZrO$_2$ storage nodes, the tunneling of electrons and holes is used for node-2 (ZrO$_2$) and node-1 (Si$_3$N$_4$) programming, respectively. The programmed $V_{th}$ increases for node-2, while it decreases for node-1. The erasing processes are converse, in that the discharging of electrons lowers the erased $V_{th}$ for node-2, while the discharging of holes increases the $V_{th}$ for node-1. As an effective F/R-read of programmed (node-2 in this paper) and overerased (node-1 in this paper) $V_{th}$’s have been reported [1]–[10], we assume that the proposed P/E scheme is feasible for the SCTL 2-b cell operation.

The band diagrams for node-2 and node-1 programming under $\pm V_g$ biases are shown in Fig. 3(a) and (b), respectively. When the electrical field ($E_{ox}$) across the 3-nm ($D_{tunnel}$) tunnel oxide exceeds $(\Delta \varphi_{c,\text{Si}} - \Delta \varphi_{c,\text{ZrO}_2})/q \times D_{tunnel} = (3.2 \text{ V} - 2.1 \text{ V})/3 \text{ nm} = 3.7 \text{ MV/cm}$, i.e., $V_g \geq 3.7 \text{ MV/cm} \times 13.3 \text{ nm} = 49.9 \text{ V}$, a direct tunneling (DT) of electrons is induced between the conduction bands of Si substrate and the ZrO$_2$ trapping layer for node-2 [13]. Whereas, a DT of electrons between the Si substrate and the Si$_3$N$_4$ trapping layer is induced when $E_{ox} > (\Delta \varphi_{c,\text{Si}} - \Delta \varphi_{c,\text{Si}_3\text{N}_4})/q \times D_{tunnel} = (3.2 \text{ V} - 1.1 \text{ V})/3 \text{ nm} = 7.0 \text{ MV/cm}$, i.e., $V_g > 7.0 \text{ MV/cm} \times 15.9 \text{ nm} = 11.2 \text{ V}$, while the modified F-N tunneling (MFNT) is induced when $V_g < 11.2 \text{ V}$. The band diagram of the SCTL device when $V_g < 11.2 \text{ V}$ is shown in Fig. 3(a), where the DT and MFNT of electrons occur for node-2 (ZrO$_2$) and node-1 (Si$_3$N$_4$), respectively. As the current density for DT ($10^{-11} - 10^{-10} \text{ A/cm}^2$) is substantially larger than that of MFNT ($10^{-17} - 10^{-12} \text{ A/cm}^2$) [13], we assume that the effect of MFNT is negligible compared with that of DT, and the tunneled electrons are trapped mainly in the ZrO$_2$ node to induce node-2 programming, without disturbing node-1 when $V_g < 11.2 \text{ V}$. On the other hand, the DT of holes occurs for Si$_3$N$_4$ when $|E_{ox}| > 6 \text{ MV/cm}$, i.e., $V_g > -6 \text{ MV/cm} \times 15.9 \text{ nm} = -9.5 \text{ V}$, while the MFNT of holes occurs for ZrO$_2$ when $|E_{ox}| < 10.5 \text{ MV/cm}$, i.e., $V_g > 10.5 \text{ MV/cm} \times 13.3 \text{ nm} = -13.9 \text{ V}$ [13].

The band diagram of the SCTL device when $V_g < -11 \text{ V}$ is shown in Fig. 3(b), where DT and MFNT of holes occur for node-1 (Si$_3$N$_4$) and node-2 (ZrO$_2$), respectively. The tunneled holes are trapped in the Si$_3$N$_4$ node to induce node-1 programming without disturbing node-2 when $V_g > -13.9 \text{ V}$. As a result, the spontaneous node control for 2-b cell programming is enabled for the SCTL devices.

The mechanisms of S/D-bias-assisted erasing for node-2 and node-1 are shown in Fig. 3(c) and (d), respectively. The effective potential ($\varphi_{eff}$) can be estimated by $\varphi_{eff} = \pm V_{d,s} + V_g$ for short-channel devices, e.g., $L_g = 250 \text{ nm}$ [16], when the S/D depletion region screens the physical storage nodes [11]. Therefore, the local $|E_{ox}|$ in the S/D screening regions can be enhanced by S/D biases so as to enable effective 2-b erasing. For example, the band diagram of the SCTL device when $V_d = 4 \text{ V}$, $V_s = -2 \text{ V}$, and $V_g \geq -8 \text{ V}$ is shown in Fig. 3(c), where electron discharging can occur for ZrO$_2$ with $|E_{ox}| < (|V_g + V_{d,s}|)/13.3 \text{ nm} = 9.0 \text{ MV/cm}$, while the disturbance to the charge storage in Si$_3$N$_4$ can be negligible with $|E_{ox}| < (|V_g - V_{s}|)/15.9 \text{ nm} = 3.7 \text{ MV/cm}$ [14]. Node-2 erasing can thus occur without disturbing node-1. Similarly, the band diagram of the SCTL device when $V_d = 2 \text{ V}$, $V_s = -4 \text{ V}$, and $V_g \leq 8 \text{ V}$ is shown in Fig. 3(d), where node-1 erasing is induced by the $V_s$-assisted hole discharging, without disturbing node-2. It is noticed that the non-uniform potential distribution in the S/D
screening regions may induce considerable erasing disturbance, which originates from the decays of surface potentials along the channel [8], [11]. With shorter channels, e.g., $L_g \leq 130$ nm, the S/D screening regions can have better surface potential control, and the erasing disturbance is expected to be better suppressed. However, the trade-off between the S/D potential control and the S/D-bias-induced short-channel effects, e.g., punchthrough or drain-induced barrier lower (DIBL), needs to be investigated.

The $V_{\text{th}}$ transient characteristics of 2-b programming for 220-nm SCTL cells are shown in Fig. 4. $V_g = 9$ to $11$ V are applied for node-2 programming. The R-read $V_{\text{th}}$’s increase from 1.63 to 2.07, 3.09, and 4.11 V for 100 ms, while they remain unchanged after being biased at $V_g = -11$ V, as shown in Fig. 4(a). In contrast, $V_g = -9$ to $-11$ V are applied for node-1 programming. The F-read $V_{\text{th}}$’s decrease from 1.57 to 0.78, 0.11, and $-0.62$ V for 100 ms, while they remain unchanged even after being biased at $V_g = 11$ V, as shown in Fig. 4(b). Distinct $V_{\text{th}}$ levels are observed for node-2 and node-1 at a reading current of $10^{-6}$ A. The feasibility of 2-b/4-level per cell operation is thus demonstrated, with negligible disturbances between the Si$_3$N$_4$ and ZrO$_2$ storage nodes. However, the operation speeds of the SCTL device need to be improved, e.g., by adopting the variable oxide thickness (VARIOT) tunnel barrier [17] and high-$\kappa$ Al$_2$O$_3$ block barrier [13] so as to enhance both the tunneling and blocking efficiency. In this paper, we demonstrated the feasibility of individual node control by $\pm V_g$ based on the DT of carriers via $\sim 3$-nm-thick SiO$_2$. However, its programming speed is not yet high enough to meet the industrial requirement of P/E operation.

The $V_{\text{th}}$ transient characteristics of 2-b erasing for the same devices are shown in Fig. 5. $V_d = 4$ V, $V_s = -2$ V, and $V_g = -6$ to $-8$ V are applied for node-2 erasing. $\varphi_{\text{eff}}$ can be $\sim 12$ V for node-2, while it is $\leq 6$ V for node-1 when $L_g$ is sufficiently small. Trapped electron discharging can thus occur for node-2 erasing, without disturbing the charge storage in node-1. The R-read $V_{\text{th}}$’s decrease from 4.39 to 3.30, 2.34, and 1.64 V for 1 s, while the F-read $V_{\text{th}}$’s remain unchanged, as shown in Fig. 5(a). It is noticed that large S/D biases, e.g., 4.5 V, can be applied to NAND circuits [3]. Fig. 5(b) shows the erasing properties for node-1 when $V_d = 2$ V, $V_s = -4$ V, and $V_g = 6$ to $8$ V are applied. The F-read $V_{\text{th}}$’s increase from $-0.64$ to 0.26, 0.85, and 1.56 V for 1 s, while
the R-read $V_{th}$’s remain unchanged. The erasing disturbances are observed for a large $\pm V_g$, i.e., node-2 erasing by $V_g \leq -8$ V induces the node-1 $V_{th}$ offset of 0.29 V, while node-1 erasing by $V_d \geq 4$ V and $V_g \geq 8$ V induces the node-2 $V_{th}$ offset of 0.41 V, as shown in Fig. 5(a) and (b), respectively. The erasing disturbances are expected to be suppressed for shorter offset of 0.29 V, as shown in Fig. 5(a) and (b), respectively. The electrical measurement results are consistent with the fine measurement results of the storage nodes in this paper. When the memory device is being programmed at $V_{ds} = 11$ V for 100 ms, the R-read $V_{th}$ is free from the second-bit effect, i.e., when the R-read $V_{th}$ after being programmed at $V_g = 11$ V for 100 ms, the F-read $\Delta V_{th} \approx 0$ V for node-1, as shown in Fig. 6(a). Similarly, the R-read $\Delta V_{th} \approx 0$ V when the F-read $\Delta V_{th} = 2.19$ V after being programmed at $V_g = 11$ V for 100 ms, as shown in Fig. 6(b). Mutual disturbances between node-2 and node-1 are effectively suppressed. The spatial charge distribution in a 220-nm SCTL is investigated by electrical measurements and the quasi-2-D model simulation [7], [8], [11]. The insets of Fig. 6(a) and (b) show the measurement and simulation results for the R/F-read currents. Assuming that the trapped electron densities are $1.5 \times 10^{12}$, $3.5 \times 10^{12}$, and $6.5 \times 10^{12}$ cm$^{-2}$, which are uniformly distributed in the 100-nm storage node apart from the channel/drain junction, and that the substrate doping density is $5 \times 10^{17}$ cm$^{-3}$, the estimated R-read $I_d$ characteristics are consistent with the electrical measurement results, as shown in the inset of Fig. 6(a). The simulated F-read $I_s$ characteristics are consistent with the measurement results when the trapped hole densities are $1.5 \times 10^{12}$, $3.0 \times 10^{12}$, and $4.5 \times 10^{12}$ cm$^{-2}$ and uniformly distributed in the 100-nm storage node, as shown in the inset of Fig. 6(b). Moreover, the subthreshold slopes remain unchanged for both node-2 and node-1 during programming, as shown in Fig. 6. This indicates that the trapped charges are well confined in the physical dimensions of the storage nodes [7].

![Image](image.png)

**Fig. 6.** Two-bit programming properties for (a) node-2 and (b) node-1 with $V_g = 9\text{–}11$ V and $-9$ to $-11$ V (Inset) Measurement and simulation results of $I_d$ and $I_s$ characteristics for node-2 and node-1 programming. The unchanged subthreshold slopes indicate well-confined charge storages for electrons in (a) and holes in (b).

**TABLE I**

<table>
<thead>
<tr>
<th>Node</th>
<th>Level</th>
<th>Pro.</th>
<th>Erase</th>
<th>$V_{th}(V)$</th>
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<tbody>
<tr>
<td>1 (Si, N$_d$)</td>
<td>$V_g(V)$</td>
<td>$V_d(V)$</td>
<td>$V_s(V)$</td>
<td>$V_{th}(V)$</td>
</tr>
<tr>
<td>11</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1.57</td>
</tr>
<tr>
<td>10</td>
<td>-9</td>
<td>2</td>
<td>-4</td>
<td>0.78</td>
</tr>
<tr>
<td>01</td>
<td>-10</td>
<td>2</td>
<td>-4</td>
<td>0.11</td>
</tr>
<tr>
<td>00</td>
<td>-11</td>
<td>2</td>
<td>-4</td>
<td>-0.62</td>
</tr>
</tbody>
</table>

For example, when the R-read $V_{th} = 11$ V, as shown in Fig. 7(a) and (b). The lateral charge-storage length $L_{st}$ is $(1.5 \times 10^{12})^{1/2} cm$, and 4.5 $(10^{12})^{1/2} cm$ and uniformly distributed in the 100-nm storage node, as shown in the inset of Fig. 6(b). Moreover, the subthreshold slopes remain unchanged for both node-2 and node-1 during programming, as shown in Fig. 6. This indicates that the trapped charges are well confined in the physical dimensions of the storage nodes [7].

**Fig. 7(a) shows the second-bit effect for the SCTL multi-bit cells with $L_g = 220$ and 250 nm. It is found that the SCTL is free from the second-bit effect, i.e., when the R-read $V_{th} = 4.29$ V for node-2, the F-read $V_{th}$’s remain at 1.59 and $-0.53$ V for node-1 under the erased and programmed states for $L_g = 220$ nm. In contrast, the second-bit effect is inevitable for NROM-type 2-b cells, i.e., the F-read $V_{th}$’s increase from $\sim 1$ to $\sim 2$ V when the R-read $V_{th} = 4.4$ V for $L_g = 430$ nm [11]. The immunity to the second-bit effect may greatly enhance the scalability of SCTL multi-bit cells.**

**Fig. 7(b) shows the lateral charge-storage length ($L_{st}$)-dependent surface potential transients which are estimated by numerical simulation based on the quasi-2-D model [11]. $L_{st}$ is used as a variable, proportional to the physical dimensions of the storage nodes in this paper. When the memory device is used as a variable, proportional to the physical dimensions of the storage nodes in this paper. When the memory device is used as a variable, proportional to the physical dimensions of the storage nodes in this paper.**

**IV. SCTL CELL SCALABILITY**

The 2-b properties for node-2 and node-1 are shown in Fig. 6(a) and (b), respectively. Excellent 2-b data clearances are maintained at both storage nodes for 220-nm SCTL devices. For example, when the R-read $\Delta V_{th} = 2.48$ V for node-2 after being programmed at $V_g = 11$ V for 100 ms, the F-read $\Delta V_{th} \approx 0$ V for node-1, as shown in Fig. 6(a). Similarly, the R-read $\Delta V_{th} \approx 0$ V when the F-read $\Delta V_{th} = 2.19$ V after being programmed at $V_g = 11$ V for 100 ms, as shown in Fig. 6(b). Mutual disturbances between node-2 and node-1 are effectively suppressed. The spatial charge distribution in a 220-nm SCTL is investigated by electrical measurements and the quasi-2-D model simulation [7], [8], [11]. The insets of Fig. 6(a) and (b) show the measurement and simulation results for the R/F-read currents. Assuming that the trapped electron densities are $1.5 \times 10^{12}$, $3.5 \times 10^{12}$, and $6.5 \times 10^{12}$ cm$^{-2}$, which are uniformly distributed in the 100-nm storage node apart from the channel/drain junction, and that the substrate doping density is $5 \times 10^{17}$ cm$^{-3}$, the estimated R-read $I_d$ characteristics are consistent with the electrical measurement results, as shown in the inset of Fig. 6(a). The simulated F-read $I_s$ characteristics are consistent with the measurement results when the trapped hole densities are $1.5 \times 10^{12}$, $3.0 \times 10^{12}$, and $4.5 \times 10^{12}$ cm$^{-2}$ and uniformly distributed in the 100-nm storage node, as shown in the inset of Fig. 6(b). Moreover, the subthreshold slopes remain unchanged for both node-2 and node-1 during programming, as shown in Fig. 6. This indicates that the trapped charges are well confined in the physical dimensions of the storage nodes [7].

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scaled down, the storage nodes and $L_e$ decrease simultaneously. We assume that the SCTL device has a substrate doping density of $5 \times 10^{17}$ cm$^{-3}$, a trapped electron density of $10^{13}$ cm$^{-3}$, an initial $V_{th}$ of 1.63 V, a read bias of 1.5 V, and $L_e$ = 60, 40, and 20 nm. The estimated surface potential transients show clear $L_e$ dependence. This suggests that the dimensions of the data nodes are successfully scaled down. Although the region where the surface potential is affected by the charge storage is much larger than $L_e$, when the DIBL characteristic length ($\zeta$) fully screens the storage node ($L_e$), the second-bit effect is suppressed [11], even when $L_e$ is down to 20 nm, as shown in the inset of Fig. 7(b). It is noticed that $\zeta$ is a function of the read bias ($V_{read}$) [11]. When $L_e$ is decreased, less $V_{read}$ provides sufficient screening to enable the 2-b data detection. For example, the $V_{read}$-dependent $\zeta$ variations are shown in Fig. 7(b) (dashed lines). It is found that $V_{read} \geq 1.5$ V is required for F/R-read when $L_e$ = 60 nm, while $V_{read} \leq 0.8$ V can enable F/R-read when $L_e$ = 20 nm. The reduced $V_{read}$ is beneficial to the short-channel-effect suppression and the device scaling. In contrast, $L_e$ is determined by the charge injection control for the NROM-type 2-b cells. As a result, $L_e$ is independent of the device structure, being a constant in the device simulation [11]. With an aggressive scaling of device dimension, i.e., when $L_g \leq 140$ nm, an overlap of $L_e$ becomes inevitable, and the 2-b operation is disabled for NROM-type devices [6], [9].

We understand that the scalability of the proposed SCTL 2-b cells is determined by the processing technologies, rather than the charge injection operations. Although S/D punchthrough during erasing poses considerable limitations to the SCTL device scaling, we think that the suppression of S/D punchthrough in short-channel devices, i.e., by using SOI substrates, is again a processing issue. In contrast, the scalability of NROM-type 2-b cells is likely pinned at 140 nm [6], due to not only the second-bit-effect but also the limitation by the large S/D biases, i.e., $V_d > 3.2$ V, required for an effective hot carrier acceleration during the P/E operations [18]. From the aforementioned viewpoints, we think that the SCTL multi-bit cell may show greater potential for future device application despite its complex operation schemes.

V. SCTL CELL RELIABILITY

Fig. 8(a) shows the endurance properties for 220-nm SCTL devices. It is found that the erased $V_{th}$ increases from ~1.6 to ~2.1 V for both node-2 and node-1, and the programmed $V_{th}$
TABLE II

<table>
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<th>Structure</th>
<th>Circuits</th>
<th>P/E mode</th>
<th>Read mode</th>
<th>Data density</th>
<th>Scalability</th>
<th>Retention</th>
<th>Endurance</th>
<th>Disturbances</th>
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<td>NAND</td>
<td>F-N/F-N</td>
<td>F/R</td>
<td>2/4-bit</td>
<td>*</td>
<td>&gt;10^9 s</td>
<td>&gt;10^5</td>
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<td>F/R</td>
<td>F/R</td>
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<td>&gt;10^9 s</td>
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*It mainly depends on the processing technology.

VI. CONCLUSION

The electrical performances and P/E mechanisms of multibit-cell Flash memory using a Si$_3$N$_4$/ZrO$_2$ SCTL have been investigated. The complementary band structure of the Si$_3$N$_4$/ZrO$_2$ storage nodes enables independent node control, and the well-confined 2-bit charge storage is accomplished by the physical data node separation. The second-bit effect is suppressed, and significant improvements in the 2-bit data clearance are enabled for short-channel SCTL devices. However, the improvement of data retention requires further investigation.

REFERENCES


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