Second-Bit-Effect-Free Multibit-Cell Flash Memory Using Si_3N_4/ZrO_2 Split Charge Trapping Layer

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***Abstract*—In this paper, a Si_3N_4/ZrO_2 split charge trapping layer (SCTL) is proposed for multibit-cell Flash memory. The complementary potential wells of Si_3N_4/ZrO_2 storage nodes enable independent node control when the Fowler–Nordheim (F–N) method is applied for programming/erasing (P/E). Experiment and simulation results suggest that the 2-bit (2-b) charge storage is accomplished by physical data node separation for the SCTL rather than charge injection control. The well-confined charge storages suppress the second-bit effect, enabling excellent 2-b data clearance for short-channel SCTL devices. It was found that the remaining memory windows after 10^5 s decrease, dependent on the difference of the trap properties between Si_3N_4 and ZrO_2.**

***Index Terms*—Flash memory, second-bit effect, Si_3N_4/ZrO_2, split charge trapping layer (SCTL).**

I. Introduction

RECENTLY, multibit-cell Flash memory based on physically separated charge-storage nodes and forward/reverse data detection (F/R-read) have been investigated extensively [1]–[5] for its great potential in future ultra-high-density data storage application [6]. However, the charge-injection-controlled multi-bit cells are rapidly approaching the scaling limits due to the second-bit effect. For example, the scalability for 2-b cells operated by channel hot electron injection (CHEI) and hot hole injection (HHI) was reported to be 110–170 nm [7]–[10]. A dual-bit high-injection MOS memory with a split Si_3N_4 trapping layer was proposed to suppress the second-bit effect. However, its scalability ($\sim$150 nm) of the split-gate devices was still limited by the source-side injection (SSI) control [5]. Moreover, the data clearance and array reliability of the 2-/4-bit cells are degraded by the second-bit-effect-induced F/R-read disturbances [11].

The second-bit effect is induced by the inefficient screening of the surface potential created by the locally injected charges [11]. For short-channel devices, the spread of charge injection results in inevitable mutual disturbances between the separated storage nodes [11]. However, it is difficult to confine the spread of CHEI/HHI [9]–[11], and the maintenance of 2-b data clearance by optimizing the CHEI/HHI profiles is critical for NROM-type devices [11]. One alternative is to realize the 2-b operation by using the F-N method based on self-initialized node control. If the stored charge is accurately confined by the physical dimension of data nodes, the charge spread can be eliminated, and the second-bit effect is expected to be suppressed.

In this paper, a Si_3N_4/ZrO_2 SCTL is proposed for second-bit-effect-free multi-bit-cell application. Si_3N_4 has small conduction band ($\Delta\varphi_c = 1.1$ eV) and large valence band ($\Delta\varphi_v = 2.6$ eV) offsets with respect to SiO_2, while ZrO_2 has a large $\Delta\varphi_c = 2.1$ eV and small $\Delta\varphi_v = 1.1$ eV [12]. The complementary band structures of Si_3N_4/ZrO_2 result in reciprocal tunneling properties for electrons and holes when the F-N method is applied for P/E, in that ZrO_2 enhances electron tunneling while it suppresses hole tunneling, whereas Si_3N_4 suppresses electron tunneling while it enhances hole tunneling [9], [13]. The independent control of Si_3N_4/ZrO_2 storage nodes by $\pm V_g$ thus becomes feasible, and the F/R-read enables a 2-b operation [1]–[3]. Experiment and simulation results suggest that charges by physical separation in the SCTL are confined better in the storage nodes, compared with those by charge injection control. With a well-confined charge storage, the second-bit effect is suppressed, and an excellent 2-b data clearance is maintained for short-channel SCTL devices. However, the improvement of data retention still requires further investigation.

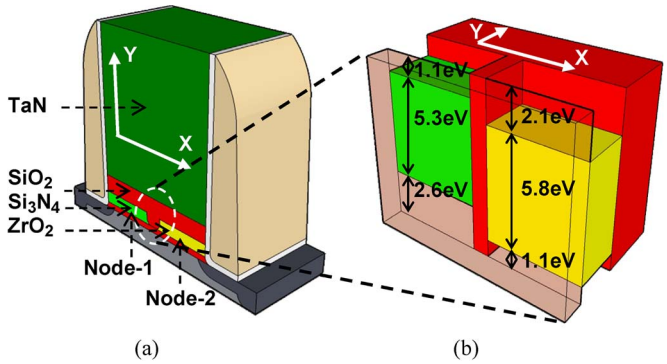

Fig. 1. Schematic of (a) the device structure and (b) the flatband diagram of the Si_3N_4/ZrO_2 SCTL, where the complementary potential wells of the SCTL are shown.

II. Device Design and Fabrication

The schematic of a device structure is shown in Fig. 1(a), and the complementary potential wells of the Si_3N_4 and ZrO_2 nodes

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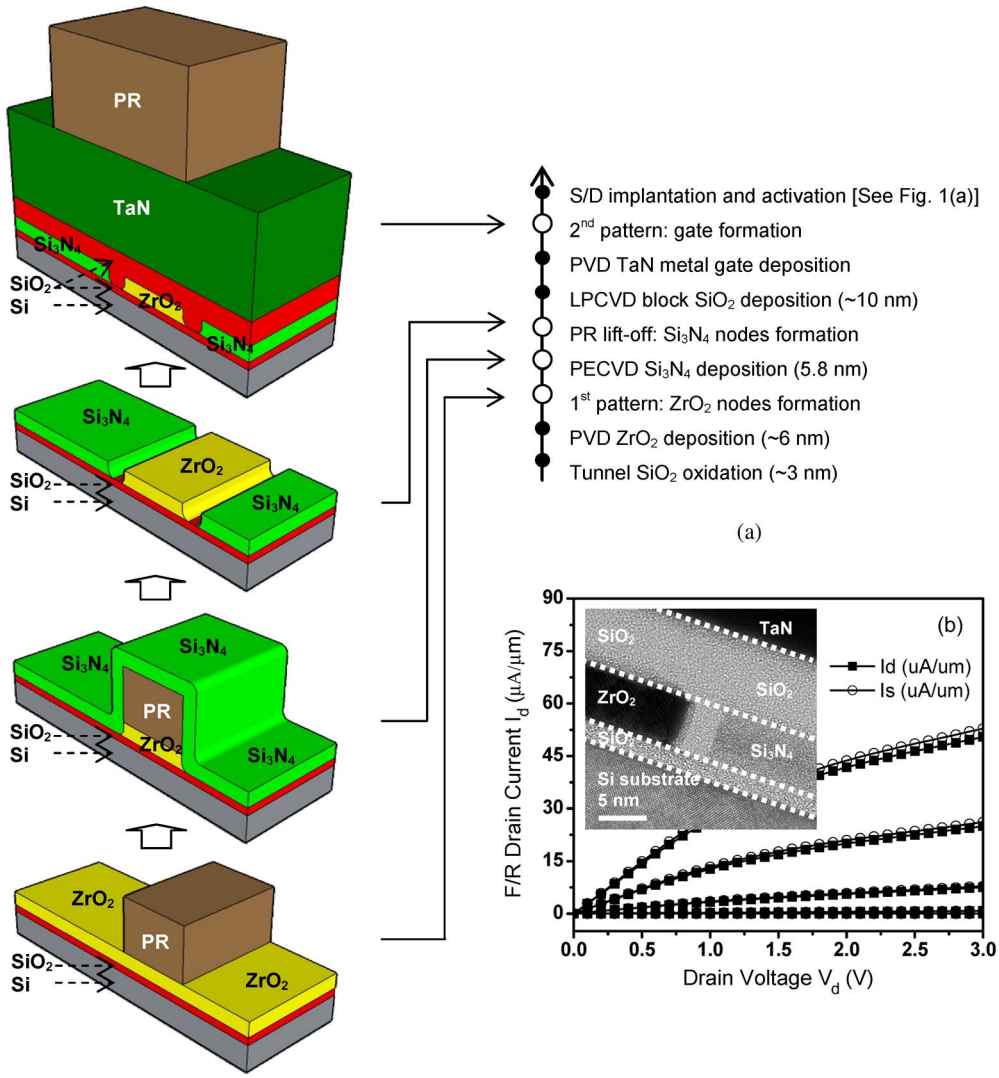

Fig. 2. (a) Illustrated process flow and (b) F/R-read I_d–V_d characteristics for a fresh SCTL device. (Inset) TEM image of the Si_3N_4/ZrO_2 SCTL gate stack.

are shown in Fig. 1(b). Si_3N_4 and ZrO_2 nodes share the channel length (L_g) to enable F/R-read at the same read biases [11], and the block oxide extension prevents the charge from migrating between the separated storage nodes. The process flow of poly-silicon–oxide–nitride–oxide–silicon (SONOS)-type devices with a Si_3N_4/ZrO_2 SCTL is shown in Fig. 2(a). After pre-gate cleaning, an about 3-nm-thick tunnel oxide (SiO_2) was thermally grown on a p-type Si substrate. Subsequently, an about 6-nm-thick ZrO_2 was deposited by the dc sputtering of Zr target in an $Ar + O_2$ ambient. After post-deposition annealing at 600 °C for 30 s, the first gate patterning was performed by a deep UV optical lithography stepper with a KrF laser source of 248-nm wavelength. After plasma etching, the ZrO_2 and the $Zr_xSi_{1-x}O_2$ interfacial layers were removed. About 5.8 nm of Si_3N_4 was then deposited by plasma-enhanced chemical vapor deposition (PECVD) to cover the formed ZrO_2 node and the remaining photoresist (PR). The Si_3N_4 layer that covers the PR (with a thickness of $\sim$0.3 μm) was removed during PR lift-off, and the split Si_3N_4/ZrO_2 charge trapping layer was formed. About 10 nm of SiO_2 was then deposited by low-pressure CVD (LPCVD) to cover the SCTL and fill the gap between the Si_3N_4/ZrO_2 nodes for the block oxide and block oxide extension formation. After an $\sim$150-nm-thick TaN gate electrode formation and the second gate patterning, As^+ was implanted with doses of 8×10^{14} cm^{-2} and 4×10^{15} cm^{-2} and energies of 10 and 35 keV for the shallow source/drain (S/D) extension and deep S/D regions, respectively, followed by activation annealing at 1000 °C for 5 s.

The formation of the gate structure with separated Si_3N_4/ZrO_2 storage nodes was confirmed by the cross-sectional transmission electron microscopy (TEM) image, as shown in the inset of Fig. 2(b). The layer thicknesses were measured by an ellipsometer during the process and confirmed by the TEM image after the device fabrication. The formation of the Si_3N_4/ZrO_2 nodes was proven by energy-dispersive X-ray spectroscopy. Good F/R-read I_d–V_d characteristics for a 220-nm fresh device which enables the reliable gate control for the SCTL gate stack are shown in Fig. 2(b). The equivalent oxide thicknesses (EOTs) of the ZrO_2 and Si_3N_4 storage stacks are estimated to be $\sim$13.3 and $\sim$15.9 nm by capacitance–voltage (C–V) measurements, respectively [14].

It is noticed that the separated storage nodes are misaligned with the gate patterning. This brings about complex fabrication and integration processes for the SCTL devices. However, the

2-b cell scalability of the SCTL devices can still be enhanced, compared with that of the NROM-type 2-b cells if the second-bit effect is suppressed. The advanced lithography technology used in the 15-nm planar memory processing presents a solution for the fabrication of short-channel SCTL devices [15]. In contrast, the scalability of the NROM-type 2-b cells is limited at 110–170 nm due to the second-bit effects, rather than the processing technologies.

III. SCTL Cell P/E Properties

Based on the complementary potential wells of the Si_3N_4/ZrO_2 storage nodes, the tunneling of electrons and holes is used for node-2 (ZrO_2) and node-1 (Si_3N_4) programming, respectively. The programmed $V_{\rm th}$ increases for node-2, while it decreases for node-1. The erasing processes are converse, in that the discharging of electrons lowers the erased $V_{\rm th}$ for node-2, while the discharging of holes increases the $V_{\rm th}$ for node-1. As an effective F/R-read of programmed (node-2 in this paper) and overerased (node-1 in this paper) $V_{\rm th}$'s have been reported [1]–[10], we assume that the proposed P/E scheme is feasible for the SCTL 2-b cell operation.

The band diagrams for node-2 and node-1 programming under $\pm V_g$ biases are shown in Fig. 3(a) and (b), respectively. When the electrical field ($E_{\rm ox}$) across the 3-nm ($D_{\rm tunnel}$) tunnel oxide exceeds $(\Delta\varphi_{c,{\rm Si}} - \Delta\varphi_{c,{\rm ZrO_2}})/q \times D_{\rm tunnel} = (3.2\ {\rm V} - 2.1\ {\rm V})/3\ {\rm nm} = 3.7\ {\rm MV/cm}$, i.e., $V_g \geq 3.7\ {\rm MV/cm} \times 13.3\ {\rm nm} = 4.9\ {\rm V}$, a direct tunneling (DT) of electrons is induced between the conduction bands of Si substrate and the ZrO_2 trapping layer for node-2 [13]. Whereas, a DT of electrons between the Si substrate and the Si_3N_4 trapping layer is induced when $E_{\rm ox} > (\Delta\varphi_{c,{\rm Si}} - \Delta\varphi_{c,{\rm Si_3N_4}})/q \times D_{\rm tunnel} = (3.2\ {\rm V} - 1.1\ {\rm V})/3\ {\rm nm} = 7.0\ {\rm MV/cm}$, i.e., $V_g > 7.0\ {\rm MV/cm} \times 15.9\ {\rm nm} = 11.2\ {\rm V}$, while the modified F-N tunneling (MFNT) is induced when $V_g < 11.2$ V. The band diagram of the SCTL device when $V_g < 11.2$ V is shown in Fig. 3(a), where the DT and MFNT of electrons occur for node-2 (ZrO_2) and node-1 (Si_3N_4), respectively. As the current density for DT ($10^{-11} - 10^{-10}$ A/cm^2) is substantially larger than that of MFNT ($10^{-17} - 10^{-12}$ A/cm^2) [13], we assume that the effect of MFNT is negligible compared with that of DT, and the tunneled electrons are trapped mainly in the ZrO_2 node to induce node-2 programming, without disturbing node-1 when $V_g < 11.2$ V. On the other hand, the DT of holes occurs for Si_3N_4 when $|E_{\rm ox}| \geq 6$ MV/cm, i.e., $V_g < -6\ {\rm MV/cm} \times 15.9\ {\rm nm} = -9.5$ V, while the MFNT of holes occurs for ZrO_2 when $|E_{\rm ox}| < 10.5$ MV/cm, i.e., $V_g > -10.5\ {\rm MV/cm} \times 13.3\ {\rm nm} = -13.9$ V [13]. The band diagram of the SCTL device when $V_g < -11$ V is shown in Fig. 3(b), where DT and MFNT of holes occur for node-1 (Si_3N_4) and node-2 (ZrO_2), respectively. The tunneled holes are trapped in the Si_3N_4 node to induce node-1 programming without disturbing node-2 when $V_g > -13.9$ V. As a result, the spontaneous node control for 2-b cell programming is enabled for the SCTL devices.

The mechanisms of S/D-bias-assisted erasing for node-2 and node-1 are shown in Fig. 3(c) and (d), respectively. The effective potential ($\varphi_{\rm eff}$) can be estimated by $\varphi_{\rm eff} = \pm V_{\rm d/s} + V_g$ for short-channel devices, e.g., $L_g = 250$ nm [16], when the S/D depletion region screens the physical storage nodes [11]. Therefore, the local $|E_{\rm ox}|$ in the S/D screening regions can be enhanced by S/D biases so as to enable effective 2-b erasing. For example, the band diagram of the SCTL device when $V_d = 4$ V, $V_s = -2$ V, and $V_g \geq -8$ V is shown in Fig. 3(c), where electron discharging can occur for ZrO_2 with $|E_{\rm ox}| < (|V_g + V_d|)/13.3\ {\rm nm} = 9.0\ {\rm MV/cm}$, while the disturbance to the charge storage in Si_3N_4 can be negligible with $|E_{\rm ox}| < (|V_g - V_s|)/15.9\ {\rm nm} = 3.7\ {\rm MV/cm}$ [14]. Node-2 erasing can thus occur without disturbing node-1. Similarly, the band diagram of the SCTL device when $V_d = 2$ V, $V_s = -4$ V, and $V_g \leq 8$ V is shown in Fig. 3(d), where node-1 erasing is induced by the V_s-assisted hole discharging, without disturbing node-2. It is noticed that the non-uniform potential distribution in the S/D

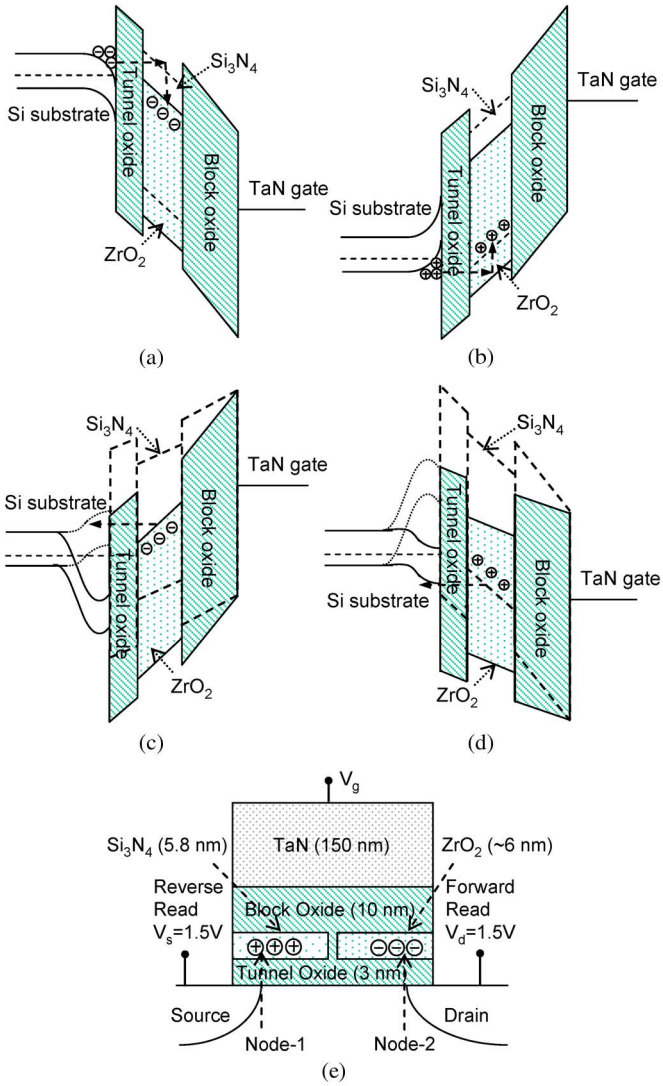

Fig. 3. Band diagrams of the SCTL device during (a) node-2 and (b) node-1 programming. Electron tunneling raises the R-read $V_{\rm th}$ for node-2, while hole tunneling decreases the F-read $V_{\rm th}$ for node-1. Band diagrams during (c) node-2 and (d) node-1 erasing. Drain-assisted electron discharging decreases the programmed $V_{\rm th}$ to the initial $V_{\rm th}$ for node-2 erasing, while source-assisted hole discharging increases the $V_{\rm th}$ for node-1 erasing. [(Dashed lines) Source/channel junction. (Solid lines) Drain/channel junction.] The bias statuses for (a)–(d) are listed in Table I. (e) F/R-read of the SCTL device for multi-bit-cell operation.

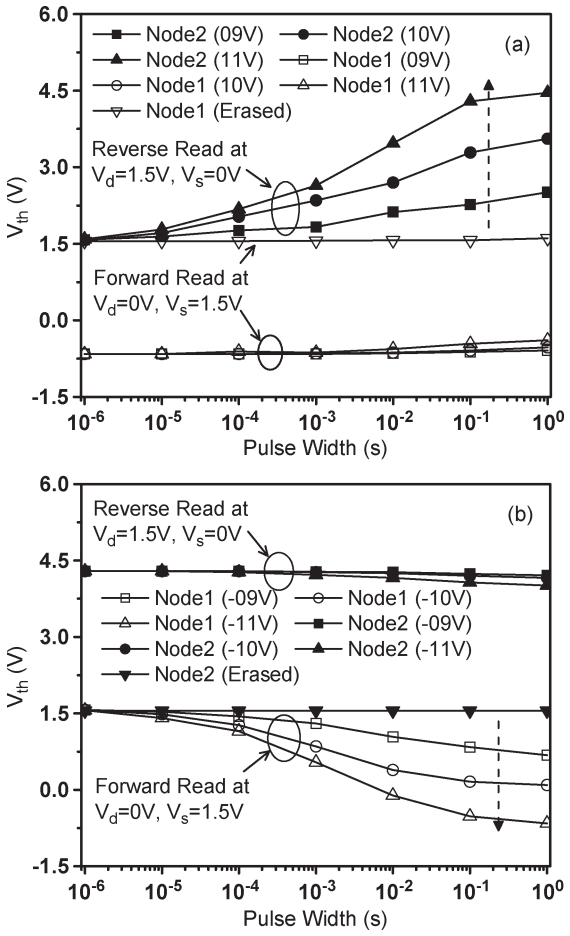

Fig. 4. $V_{\rm th}$ transients for (a) node-2 programming by $V_g = 9{-}11$ V and (b) node-1 programming by $V_g = -9$ to -11 V. Negligible mutual disturbances are observed for node-2 and node-1 programming.

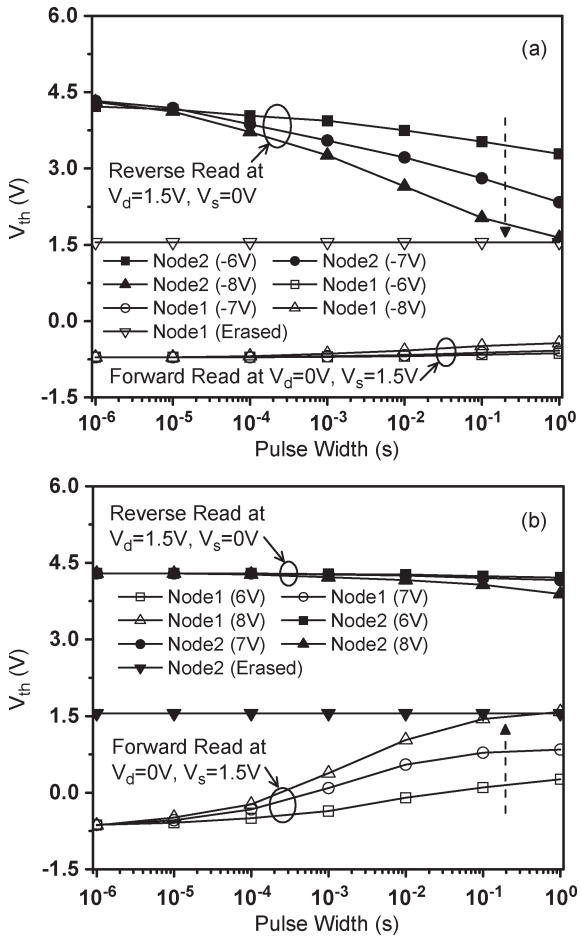

Fig. 5. $V_{\rm th}$ transients for (a) node-2 erasing at $V_d = 4$ V, $V_s = -2$ V, and $V_g = -6$ to -8 V, and (b) node-1 erasing at $V_d = 2$ V, $V_s = -4$ V, and $V_g = 6{-}8$ V. Negligible mutual disturbances are observed when -8 V $\leq V_g \leq 8$ V for node-2 and node-1 erasing.

screening regions may induce considerable erasing disturbance, which originates from the decays of surface potentials along the channel [8], [11]. With shorter channels, e.g., $L_g \leq 130$ nm, the S/D screening regions can have better surface potential control, and the erasing disturbance is expected to be better suppressed. However, the trade-off between the S/D potential control and the S/D-bias-induced short-channel effects, e.g., punchthrough or drain-induced barrier lower (DIBL), needs to be investigated. Fig. 3(e) shows the schematic diagram for F/R-read of the 2-b SCTL device. With well-confined charge storage and sufficient S/D screening, the complementary charge storages are unlikely to induce significant read disturbances for short-channel SCTL devices [11].

The $V_{\rm th}$ transient characteristics of 2-b programming for 220-nm SCTL cells are shown in Fig. 4. $V_g = 9{-}11$ V are applied for node-2 programming. The R-read $V_{\rm th}$'s increase from 1.63 to 2.07, 3.09, and 4.11 V for 100 ms, while they remain unchanged after being biased at $V_g = -11$ V, as shown in Fig. 4(a). In contrast, $V_g = -9$ to -11 V are applied for node-1 programming. The F-read $V_{\rm th}$'s decrease from 1.57 to 0.78, 0.11, and -0.62 V for 100 ms, while they remain unchanged even after being biased at $V_g = 11$ V, as shown in Fig. 4(b). Distinct $V_{\rm th}$ levels are observed for node-2 and node-1 at a reading current of 10^{-6} A. The feasibility of 2-b/4-level per cell operation is thus demonstrated, with negligible disturbances between the Si_3N_4 and ZrO_2 storage nodes. However, the operation speeds of the SCTL device need to be improved, e.g., by adopting the variable oxide thickness (VARIOT) tunnel barrier [17] and high-κ Al_2O_3 block barrier [13] so as to enhance both the tunneling and blocking efficiency. In this paper, we demonstrated the feasibility of individual node control by $\pm V_g$ based on the DT of carriers via $\sim$3-nm-thick SiO_2. However, its programming speed is not yet high enough to meet the industrial requirement of P/E operation.

The $V_{\rm th}$ transient characteristics of 2-b erasing for the same devices are shown in Fig. 5. $V_d = 4$ V, $V_s = -2$ V, and $V_g = -6$ to -8 V are applied for node-2 erasing. $\varphi_{\rm eff}$ can be $\sim$12 V for node-2, while it is ≤ 6 V for node-1 when L_g is sufficiently small. Trapped electron discharging can thus occur for node-2 erasing, without disturbing the charge storage in node-1. The R-read $V_{\rm th}$'s decrease from 4.39 to 3.30, 2.34, and 1.64 V for 1 s, while the F-read $V_{\rm th}$'s remain unchanged, as shown in Fig. 5(a). It is noticed that large S/D biases, e.g., 4.5 V, can be applied to NAND circuits [3]. Fig. 5(b) shows the erasing properties for node-1 when $V_d = 2$ V, $V_s = -4$ V, and $V_g = 6{-}8$ V are applied. The F-read $V_{\rm th}$'s increase from -0.64 to 0.26, 0.85, and 1.56 V for 1 s, while

TABLE I
OPERATION SCHEMES AND THE RESULTING $V_{\rm th}$ LEVELS

Node	Level	Pro.	Erase			$V_{\rm th}$(V)
1 (Si_3N_4)		$V_{\rm g}$(V)	$V_{\rm d}$ (V)	$V_{\rm s}$ (V)	$V_{\rm g}$ (V)	$V_{\rm s}$=1.5V
	11	0	0	0	0	1.57
	10	–9	2	–4	6	0.78
	01	–10	2	–4	7	0.11
	00	–11	2	–4	8	−0.62
2 (ZrO_2)		$V_{\rm g}$(V)	$V_{\rm d}$(V)	$V_{\rm s}$(V)	$V_{\rm g}$(V)	$V_{\rm d}$=1.5V
	11	0	0	0	0	1.63
	10	9	4	–2	–6	2.07
	01	10	4	–2	–7	3.09
	00	11	4	–2	–8	4.11

the R-read $V_{\rm th}$'s remain unchanged. The erasing disturbances are observed for a large $\pm V_g$, i.e., node-2 erasing by $V_g \leq -8$ V induces the node-1 $V_{\rm th}$ offset of 0.29 V, while node-1 erasing by $V_d \geq 4$ V and $V_g \geq 8$ V induces the node-2 $V_{\rm th}$ offset of 0.41 V, as shown in Fig. 5(a) and (b), respectively. The erasing disturbances are expected to be suppressed for shorter channel devices. It is also noticed that the channel is turned on during the node-1 erasing. However, the effects of CHEI can be negligible to node-2, as $V_d = 2$ V is insufficient for hot electron acceleration [9]. However, the large drain leakage which originates from the forward biased source ($V_s = -4$ V) seems inevitable, unless the S/D biases can be reduced by tunnel barrier engineering. In this paper, the drain leakage during node-1 erasing was found to be $I_d \approx 64$ mA/μm, which is $\sim 10^3$ times larger compared with that ($\sim$50 μA/μm) under a normal operation ($V_s = 0$ V) in Fig. 2(b). We assume that the SCTL device may be erased by bit/byte erasing, rather than block erasing. Table I lists the P/E schemes and the resulting $V_{\rm th}$ levels for the SCTL multi-bit cells during 2-b/4-level per cell operation.

IV. SCTL CELL SCALABILITY

The 2-b properties for node-2 and node-1 are shown in Fig. 6(a) and (b), respectively. Excellent 2-b data clearances are maintained at both storage nodes for 220-nm SCTL devices. For example, when the R-read $\Delta V_{\rm th} = 2.48$ V for node-2 after being programmed at $V_g = 11$ V for 100 ms, the F-read $\Delta V_{\rm th} \approx 0$ V for node-1, as shown in Fig. 6(a). Similarly, the R-read $\Delta V_{\rm th} \approx 0$ V when the F-read $\Delta V_{\rm th} = 2.19$ V after being programmed at $V_g = -11$ V for 100 ms, as shown in Fig. 6(b). Mutual disturbances between node-2 and node-1 are effectively suppressed. The spatial charge distribution in a 220-nm SCTL is investigated by electrical measurements and the quasi-2-D model simulation [7], [8], [11]. The insets of Fig. 6(a) and (b) show the measurement and simulation results for the R/F-read currents. Assuming that the trapped electron densities are 1.5×10^{12}, 3.5×10^{12}, and 6.5×10^{12} cm^{-2}, which are uniformly distributed in the 100-nm storage node apart from the channel/drain junction, and that the substrate doping density is 5×10^{17} cm^{-3}, the estimated R-read I_d characteristics are consistent with the electrical measurement results, as shown in the inset of Fig. 6(a). The simulated F-read

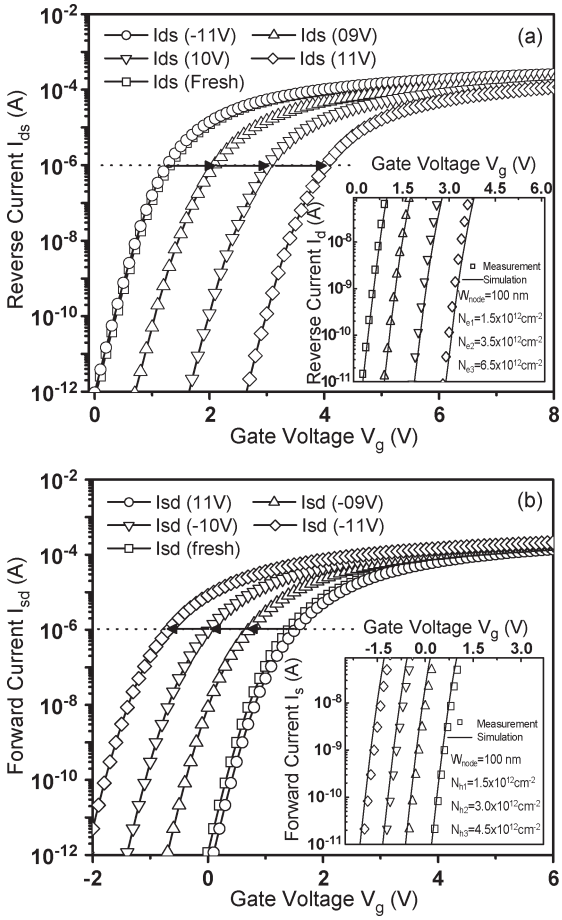

Fig. 6. Two-bit programming properties for (a) node-2 and (b) node-1 with $V_g = 9-11$ V and -9 to -11 V. (Inset) Measurement and simulation results of I_d and I_s characteristics for node-2 and node-1 programming. The unchanged subthreshold slopes indicate well-confined charge storages for electrons in (a) and holes in (b).

I_s characteristics are consistent with the measurement results when the trapped hole densities are 1.5×10^{12}, 3.0×10^{12}, and 4.5×10^{12} cm^{-2} and uniformly distributed in the 100-nm storage node, as shown in the inset of Fig. 6(b). Moreover, the subthreshold slopes remain unchanged for both node-2 and node-1 during programming, as shown in Fig. 6. This indicates that the trapped charges are well confined in the physical dimensions of the storage nodes [7].

Fig. 7(a) shows the second-bit effect for the SCTL multi-bit cells with $L_g = 220$ and 250 nm. It is found that the SCTL is free from the second-bit effect, i.e., when the R-read $V_{\rm th} = 4.29$ V for node-2, the F-read $V_{\rm th}$'s remain at 1.59 and -0.53 V for node-1 under the erased and programmed states for $L_g = 220$ nm. In contrast, the second-bit effect is inevitable for NROM-type 2-b cells, i.e., the F-read $V_{\rm th}$'s increase from $\sim$1 to $\sim$2 V when the R-read $V_{\rm th} = 4.4$ V for $L_g = 430$ nm [11]. The immunity to the second-bit effect may greatly enhance the scalability of SCTL multi-bit cells.

Fig. 7(b) shows the lateral charge-storage length (L_e)-dependent surface potential transients which are estimated by numerical simulation based on the quasi-2-D model [11]. L_e is used as a variable, proportional to the physical dimensions of the storage nodes in this paper. When the memory device is

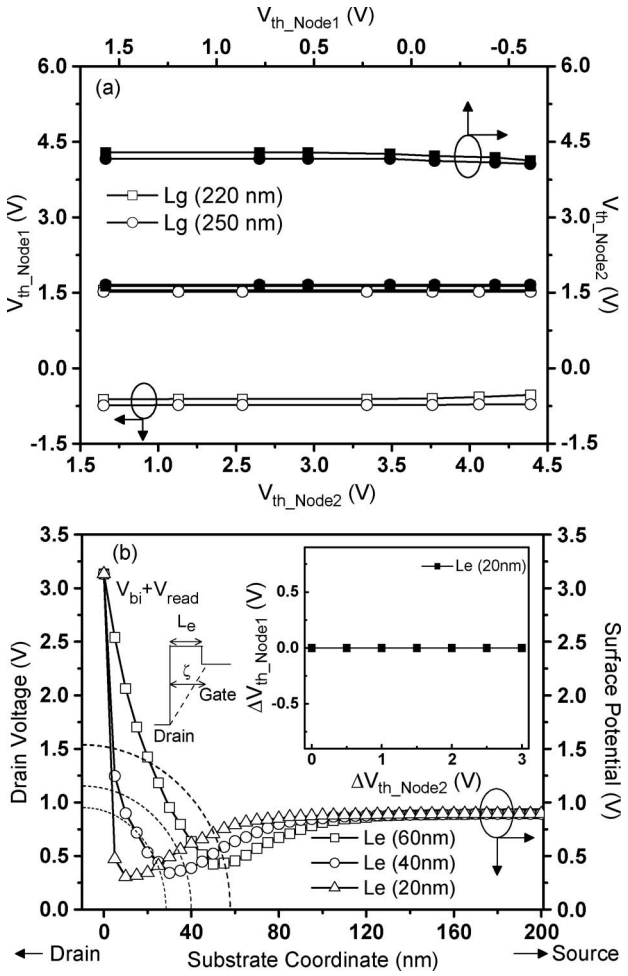

Fig. 7. (a) Second-bit effects for the SCTL 2-b cells with $L_g = 220-250$ nm. (b) The estimated surface potential transients induced by different lateral charge spreads with (solid lines) $L_e = 20-60$ nm and (dashed lines) the estimated DIBL characteristic length (ζ). (Inset) The estimated second-bit effect for an SCTL 2-b cell with 20-nm storage nodes.

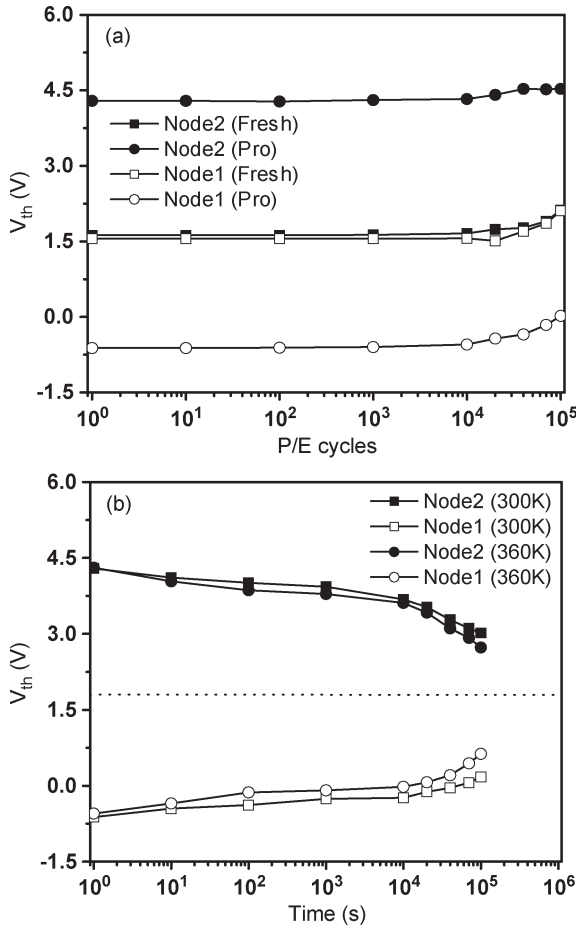

Fig. 8. (a) Two-bit endurance and (b) retention properties for the SCTL devices.

scaled down, the storage nodes and L_e decrease simultaneously. We assume that the SCTL device has a substrate doping density of 5×10^{17} cm^{-3}, a trapped electron density of 10^{13} cm^{-3}, an initial $V_{\rm th}$ of 1.63 V, a read bias of 1.5 V, and $L_e = 60$, 40, and 20 nm. The estimated surface potential transients show clear L_e dependence. This suggests that the dimensions of the data nodes are successfully scaled down. Although the region where the surface potential is affected by the charge storage is much larger than L_e, when the DIBL characteristic length (ζ) fully screens the storage node (L_e), the second-bit effect is suppressed [11], even when L_e is down to 20 nm, as shown in the inset of Fig. 7(b). It is noticed that ζ is a function of the read bias $(V_{\rm read})$ [11]. When L_e is decreased, less $V_{\rm read}$ provides sufficient screening to enable the 2-b data detection. For example, the $V_{\rm read}$-dependent ζ variations are shown in Fig. 7(b) (dashed lines). It is found that $V_{\rm read} \geq 1.5$ V is required for F/R-read when $L_e = 60$ nm, while $V_{\rm read} \leq 0.8$ V can enable F/R-read when $L_e = 20$ nm. The reduced $V_{\rm read}$ is beneficial to the short-channel-effect suppression and the device scaling. In contrast, L_e is determined by the charge injection control for the NROM-type 2-b cells. As a result, L_e is independent of the device structure, being a constant in the device simulation [11]. With an aggressive scaling of device dimension, i.e., when $L_g \leq 140$ nm, an overlap of L_e becomes inevitable, and the 2-b operation is disabled for NROM-type devices [6], [9].

We understand that the scalability of the proposed SCTL 2-b cells is determined by the processing technologies, rather than the charge injection operations. Although S/D punchthrough during erasing poses considerable limitations to the SCTL device scaling, we think that the suppression of S/D punchthrough in short-channel devices, i.e., by using SOI substrates, is again a processing issue. In contrast, the scalability of NROM-type 2-b cells is likely pinned at 140 nm [6], due to not only the second-bit-effect but also the limitation by the large S/D biases, i.e., $V_d > 3.2$ V, required for an effective hot carrier acceleration during the P/E operations [18]. From the aforementioned viewpoints, we think that the SCTL multi-bit cell may show greater potential for future device application despite its complex operation schemes.

V. SCTL Cell Reliability

Fig. 8(a) shows the endurance properties for 220-nm SCTL devices. It is found that the erased $V_{\rm th}$ increases from ~1.6 to ~2.1 V for both node-2 and node-1, and the programmed $V_{\rm th}$

TABLE II
COMPARISON OF THIS WORK TO THE OTHER WORKS

References	This work	IEDM 2006, p547 [2]	VLSI 2005, p116 [3]	IEDM 2006, p967 [4]	TED v52n10 p2250, 05 [5]
Structure	SCTL	NROM	PHINES	DSM	Bi-HIMOS
Circuits	NAND	NOR	NAND	NOR	NOR
P/E mode	F-N/F-N	CHEI/HHI	IIHEI/HHI	CHEI/HHI	SSI/HHI
Read mode	F/R	F/R	F/R	F/R	F/R
Data density	2/4-bit	4-bit	2-bit	4-bit	2-bit
Scalability	*	-	120 nm	120 nm	150 nm
Retention	$>10^6$s	-	$>10^5$s	10^6s	10^8s
Endurance	$>10^5$	10^4	$>10^4$	$>10^5$	10^4
Disturbances	Read	P/E	Read	P/E	P/E

*it mainly depends on the processing technology.

increases from 4.29 to 4.53 V for node-2 and from -0.62 to 0.02 V for node-1 throughout the 10^5 P/E cycles. Different from the other charge-injection-controlled multi-bit cells [1]–[5], the SCTL devices are immune to the channel charge accumulation induced by charge-injection mismatches [7]–[9], as they are operated by the F-N method. Moreover, the block oxide extension isolates the Si_3N_4/ZrO_2 storage nodes, preventing the stored charge from accumulating or migrating. Therefore, the endurance reliability of the SCTL 2-b cells is efficiently improved. Nevertheless, $V_{\rm th}$ increases are still observed for the SCTL devices after 10^4 P/E cycles due to the trap generation in tunnel oxide induced by the $\pm V_g$ stress [2]. Fig. 8(b) shows the 2-b charge retention at 300 and 360 K after 10^5 P/E cycling. The remaining memory windows are 1.39 and 1.46 V for node-2 and node-1 after 10^5 s at 300 K, while they are 1.11 and 1.02 V at 360 K. We understand that the $V_{\rm th}$ decays are attributed to the DT of the trapped charges via the ultra-thin tunnel oxide, and the temperature dependences reflect the divergence in the trap properties between Si_3N_4 and ZrO_2. It is possible to apply the band-engineered tunnel barrier or trap engineering to improve the data retention property for the SCTL devices. For example, the ONO- [19] or $SiO_2/Hf_xSi_{1-x}O_2/SiO_2$-type band-engineered tunnel barrier may be adopted to achieve the VARIOT application [17], so that the DT of carriers during the retention mode can be substantially suppressed [13]. Moreover, trap engineering may suppress the trapped charge discharging so as to improve the retention reliability [20]. However, the processing issues of the band-engineered tunnel barrier still require further investigation, e.g., the thermal instability of the ultra-thin layers [9], the unwanted interfacial layer formation [18], etc. The performances of the SCTL devices are compared with the other works in Table II.

VI. CONCLUSION

The electrical performances and P/E mechanisms of multi-bit-cell Flash memory using a Si_3N_4/ZrO_2 SCTL have been investigated. The complementary band structure of the Si_3N_4/ZrO_2 storage nodes enables independent node control, and the well-confined 2-b charge storage is accomplished by the physical data node separation. The second-bit effect is suppressed, and significant improvements in the 2-b data clearance are enabled for short-channel SCTL devices. However, the improvement of data retention requires further investigation.

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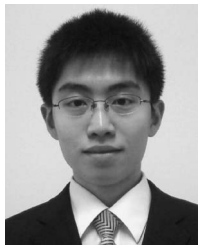

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