

Potential Well Engineering by Partial Oxidation of TiN for High-Speed and Low-Voltage Flash Memory with Good 125°C Data Retention and Excellent Endurance

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ABSTRACT

Potential well engineering is proposed for NAND Flash memory. With a variable (~2nm-4.3nm) tunnel barrier, the engineered well (EW) enhances tunneling of carriers during program/erase (P/E) to result in fast P/E, while it suppresses charge loss under the retention mode to result in good data retention. The EW also improves endurance, as it is insensitive to the P/E stress induced tunnel barrier degradation. The EW demonstrated in this work is formed by partial oxidation of TiN at the interfaces of the SiO₂/TiN/SiO₂ stack during rapid thermal process (RTP), and its band profile is characterized by XPS, TEM, internal photoemission (IPE), XRD, and band simulation. The memory devices with an EW show promising performances in fast program (<μs), low-voltage operation (6-8MV/cm), good 10-year data retention at 125°C, and excellent endurance (>10⁷ P/E cycles).

INTRODUCTION

Enhanced tunneling of carriers during P/E and suppressed charge loss under the retention mode enable fast P/E and good data retention for the SONOS Flash memories with an engineered-tunnel-barrier (ETB) [1-4]. The fast P/E and good data retention can also be accomplished by the potential well engineering, as shown in Fig. 1: (a) The EW has transitional boundaries between the tunnel/block barriers, and deep traps are located at the bottom of EW. (b, c) During P/E operations, the EW is bent by the gate electric field ($\pm E_{ox}$), and direct-tunneling (DT) of carriers via the shrunk tunnel barrier occurs to enable fast P/E. (d) Under the retention mode, the EW is transformed due to charge trapping. The deep traps and the enlarged tunnel barrier suppress charge loss, leading to good data retention. Different from the ETBs, the tunnel barrier thickness is varied by the transformation of the EW (see Fig. 1), rather than by the modulation of the ETBs [1-4]. Thus, (i) the EW switches the P/E and retention modes more effectively, as the EW (trapping layer) is bent by $\pm E_{ox}$ more efficiently than both the trapping layer and the ETBs, and (ii) the EW is insensitive to the stress induced tunnel barrier degradation during the P/E cycling.

A Flash cell with an EW (merged trapping layer) is shown in Fig. 2. The EW is formed by partial oxidation of TiN. Thin (~6nm) TiN film deposited at low-temperature (600°C) is structurally irregular and thermodynamically non-equilibrium [5]. It interacts with SiO₂ [6] to form ~3nm TiO_xN_y and ~1nm SiO_xN_y transition layers during RTP at 900°C. The transition layers form the EW, and its band profile is inferred by XPS, IPE and band simulation [7]. At the bottom of the EW, TiN nanocrystal trapping sites [8] are detected by TEM and XRD. The memory devices with an EW show faster program (<μs) and improved endurance (>10⁷ P/E cycles) compared to those with an ETB (~10²μs / >10⁵ P/E cycles) in [2-4]. Moreover, the simple structure of the EW is also advantageous in process control and device scaling.

EXPERIMENTS AND ANALYSES

Memory devices with a Si/SiO₂/TiN/SiO₂/TaN (SOTOT: -/3/6/9/150nm) gate stack were fabricated by standard CMOS process. About 3-nm-thick tunnel oxide was first thermally grown at 875°C on a p-type silicon wafer. Subsequently, ~6-nm-thick TiN layer was deposited on SiO₂ by e-beam evaporation using a TiN target at 600°C. The TiN layer was then capped with a 9-nm-thick block oxide formed by low-pressure chemical vapor deposition (LPCVD). About 150-nm-thick TaN was deposited by sputtering of a Ta target in an Ar+N₂ ambient, and patterned as the gate electrode, followed by ion implantation (As⁺, 1×10¹⁵ cm⁻², 70keV). Thicknesses of the layers were measured by an ellipsometer. Activation annealing was performed by RTP at 900°C for 10s to form the source/drain (S/D) regions, and followed by forming gas annealing at 420°C. The pre-deposited TiN interacts with the bottom and the top SiO₂ during RTP [6] to form the EW. The experimental flow is shown in Table 1.

Reference samples (#1)(Si/SiO₂/TiN: -/3/5nm) and (#2)(Si/TiO_xN_y(or SiO₂)/TaN: -/5/9nm, x=0.44-2, y=1-0.11) were also fabricated, after undergoing 900°C RTP at vacuum for 10s. XPS surface profiling performed on the reference samples (#1) suggests the formation of TiO_xN_y and SiO_xN_y transition layers from the presence of Ti-O-N and Si-O-N bonds, as shown in Fig. 3. XPS depth profiling indicates that the thickness of TiO_xN_y is ~3nm, while that of SiO_xN_y is ~1nm [9], as shown in Fig. 4. By fitting the XPS spectra of the Ti- and Si-bonds at various depths in Fig. 4 with those obtained from the reference samples (#2), the XPS spectra at the depths of 2nm/1nm/0nm are found to correspond to those obtained from TiO_{0.76}N_{0.71}/TiO_{1.04}N_{0.66}/TiO_{1.36}N_{0.60}, and this leads us to infer the phase transitions of TiO_xN_y and SiO_xN_y in the depth range from 3nm -(~1nm) [7], as shown in (Left) Fig. 5. The estimated phase transitions correspond to the cross-sectional TEM results of the OTO stack, as shown in (Right) Fig. 5. Fig. 5 (circled) also shows crystalline TiN of ~1nm. In Fig. 6, XRD analyses performed on the reference samples (#1) before and after RTP confirm the formation of TiN nanocrystals.

IPE tests were performed to estimate the band offsets of TiO_xN_y [5]. The principle of IPE is described pictorially in the insets of Fig. 7. The transition of the photo-excited carriers across the TiO_xN_y barrier is induced when appropriate optical energy ($h\nu > \Phi$) is supplied, where h is the Planck constant, ν is the photon frequency, and Φ is the work function between the valance/conduction bands of Si and TiO_xN_y. By detecting the photo-excited carrier flux, the corresponding $h\nu$ and Φ are estimated. The photo-conductivity transients are shown in Fig. 7, and the extracted band offsets of TiO_xN_y to Si are shown in Fig. 8 (shown as dots). Surface resistivity of TiO_{0.61}N_{0.78} at the depth of 3nm in Fig. 4 is ~10⁵-10⁶ Ωcm. This ensures the validity of the IPE results. By aligning the band offsets of TiO_xN_y and SiO_xN_y to SiO₂, the band diagram of the OTO gate stack is built [7], as shown in (solid lines) Fig. 8. The

experimental and simulation results indicate that an EW is formed, with the conduction and valance band offsets to SiO₂ ($\Delta\varphi_c$ and $\Delta\varphi_v$) of ~3.8eV and ~3.8eV at the bottom of the EW, where the TiN nanocrystal ($\Delta\varphi_c \approx 4.5$ eV [10]) trapping levels are located.

ELECTRICAL PERFORMANCES

Equivalent oxide thickness (EOT) of the SOTOT device is ~13nm, estimated by CV measurements. The P/E electric field, $\pm E_{ox}$, is $\pm V_g/\text{EOT}$. Fig. 9 shows the gate leakages of the SOTOT and SONOS devices. It is found that tunneling of electrons is enhanced for the SOTOT device compared to the SONOS device at $E_{ox}=6-10\text{MV}/\text{cm}$. The enhanced tunneling of electrons leads to fast program at low-voltage operations [1,2,4]. Fig. 10 shows good I_d-V_d and I_d-V_g characteristics for a SOTOT device. ΔV_{th} is read by the I_d shifts before and after program. The ΔV_{th} transients induced by various E_{ox} (2-10 MV/cm) and pulse widths ($10^{-9}\text{s}-10^{-3}\text{s}$) are shown in Fig. 11. Compared with the SONOS devices with a Si₃N₄ and ZrO₂ trapping layer, the SOTOT device shows faster program speed (<μs) at low-voltage operations (6-8MV/cm). Meanwhile, the program speed of the SOTOT devices is also largely enhanced compared with that of the SONOS devices with an ETB, as listed in Table 2. This can be attributed to higher efficiency of E_{ox} control during the P/E operations using the EW compared to that using the ETBs: the $\pm E_{ox}$ bends only the trapping layer to enhance tunneling of carriers during P/E for the EW device, while it bends both the trapping layer and the ETB to enable P/E, and then the modulation of the ETB enhances tunneling of carriers for the ETB devices [1-4]. On the other hand, the tunnel barrier of the EW is insignificantly stressed during the P/E cycling, thus the EW is insensitive to P/E stress induced tunnel barrier degradation, and endurance of the EW can be improved.

The P/E and endurance properties of a SOTOT device are shown in Fig. 12. Clear V_{th} control is maintained throughout the 10^7 P/E cycles. Cumulative distribution of V_{th} windows is shown in Fig. 13. Uniform V_{th} windows are maintained for 14 SOTOT devices which had undergone 10^7 P/E cycles. Read disturbance at $V_g=\pm 5.2\text{V}$ ($E_{ox}=\pm 4\text{MV}/\text{cm}$) is negligible even after the 10^7 P/E cycling, as shown in Fig. 14. Note that multi-level operation may be applicable to the SOTOT devices with clear multi-level V_{th} control throughout the 10^7 P/E cycling, as shown in Fig. 12.

The accelerated data retentions of a fresh SOTOT device at 100°C-300°C (dots) and the V_{th} decay transients estimated by the F-N model (solid lines) [11] are shown in Fig. 15(a). The F-N model is based on complete F-N current calculation for charge trapped ONO stack. Assume that the internal electric field between the charge trapping layer and the grounded Si substrate is $E_{ox}(t)=Q(t)/C_{ox}=[V_{th}(t)-V_{th}(0)]/D_{tunnel}$, where $Q(t)$ is the trapped charge density, C_{ox} is the capacitance of the tunnel barrier, D_{tunnel} is the thickness of tunnel barrier, t is the duration under retention, and initial $V_{th}(0)=1.32\text{V}$. Meanwhile, F-N tunneling of the trapped charges via the tunnel barrier to Si substrate is induced by $E_{ox}(t)$, and the leakage current can be calculated by $J_{leak}=dQ(t)/dt$. Thus,

$$t = (\varepsilon_0 \varepsilon_{ox} / \alpha) \int_{E_{ox}(0)}^{E_{ox}(t)} [df / J_{leak}(f, T)],$$

where $\varepsilon_0=8.854 \times 10^{-14} \text{ F}/\text{cm}$, ε_{ox} is the relative permittivity of SiO₂ of 3.9, T is the temperature, and $E_{ox}(0)$ is the electric field via the tunnel barrier at the uncharged state [11]. On the

other hand, $t=t_0 \cdot \exp[-T/T_0]$, where t_0 and T_0 are the reference duration and the corresponding temperature, respectively [11]. In this work, we use $t_0=3 \times 10^3$ hours, $T_0=175^\circ\text{C}$, and assume $\alpha=6.5 \times 10^{-4} \text{ eV}/\text{K}$. It is found that the measured ΔV_{th} decays (dots) correspond to the simulation results (solid lines) by assuming $D_{tunnel}=3.7\text{nm}, 4.0\text{nm}, 4.3\text{nm}$, and 4.3nm at 300°C , 250°C , 200°C , and 150°C , respectively. The programmed V_{th} (~3.74V) decays by ~0.81V during the 1st hour, and the V_{th} decays then follow the F-N model [11] during the subsequent 99 hours baking. It is likely that the rapid V_{th} decay during the 1st hour is induced by discharging of the SiO_xN_y shallow traps at the boundary of EW (see Fig. 8). The deep traps of TiN (4.5eV) and the enlarged tunnel barrier (3.7nm-4.3nm) under the retention mode then suppress charge loss (see Fig. 1), giving rise to good data retention at up to 125°C . Charge loss and thereby the V_{th} decays at 200°C are enhanced by trap assisted tunneling over the 10^7 P/E cycles, as shown in Fig. 15(b). However, the EW still maintains good 10-year data retentions after 10^7 P/E cycles at 75°C and 125°C , as shown in Fig. 16.

CONCLUSION

Potential well engineering is proposed for NAND Flash memory. The EW is formed by partial oxidation of TiN, and its band diagram is built by physical characterization and band simulation. The EW enhances tunneling of carriers during P/E, while it suppresses charge loss under the retention mode. Moreover, the EW is insensitive to P/E stress induced tunnel barrier degradation. Thus, the memory devices with an EW show promising performances in fast P/E, good retention, and excellent endurance.

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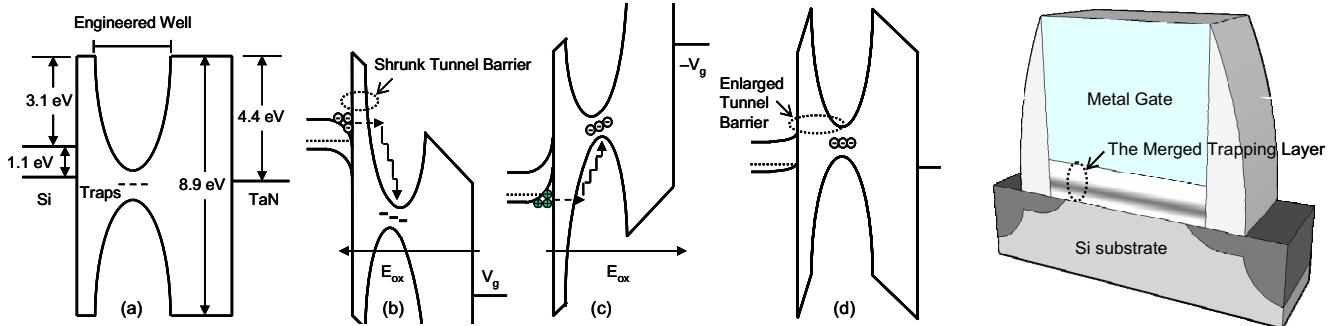


Fig. 1: Band diagrams of an engineered well (EW) (a) under flat band, (b,c) during P/E and (d) under retention mode. The EW has transitional boundaries and deep trapping levels in (a). When $\pm E_{ox} = \pm V_g / EOT$ is applied, direct tunneling of electrons/holes via the shrunk tunnel barrier is induced in (b) and (c). The trapped charge raises the bottom of EW, so that reverse tunneling is suppressed by the enlarged tunnel barrier in (d). The tunnel barrier of the EW is insignificantly stressed by $\pm E_{ox}$ in (b) and (c).

Fig. 2: Schematic of a Flash memory device with an EW. The charge trapping layer merges with the tunnel/block barriers to form the transition layers, and the band diagrams of the transition layers form the EW.

Table 1. Experimental flow

1. Thermal growth of 3nm SiO_2
2. Deposition of ~6nm TiN by e-beam evaporation at 600°C
3. 9nm SiO_2 deposition by LPCVD
4. 150nm TaN deposition by PVD
5. Gate formation
6. Source/Drain (S/D) implantation
7. RTP at vacuum at 900°C for 10s for EW formation and S/D activation
8. Forming gas annealing at 420°C
9. Reference samples (#1) ($\text{Si}/\text{SiO}_2/\text{TiN}$: -3/5nm) preparation by steps 1,2,7
10. Reference samples (#2) ($\text{Si}/\text{TiO}_x\text{N}_y$ (or SiO_2)/TaN: -5/9nm) preparation by steps 1,2,4,7 (step 2 is by reactive PVD)
11. XPS, TEM, XRD, and IPE analyses
12. Band diagram simulation
13. Electrical characterization

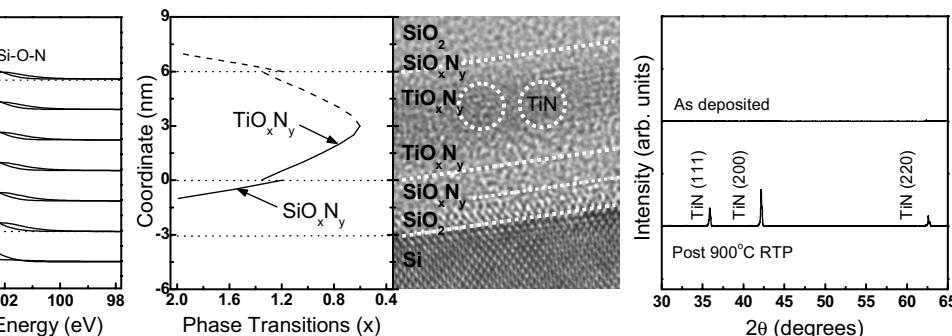
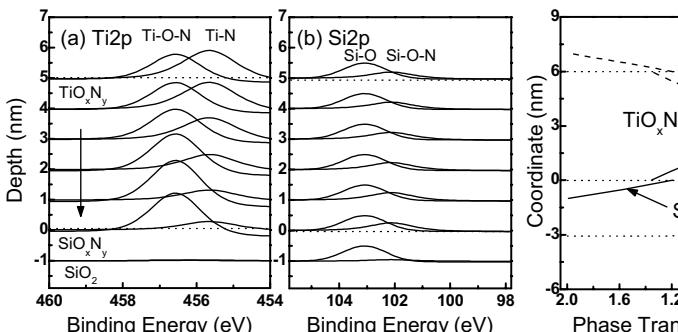
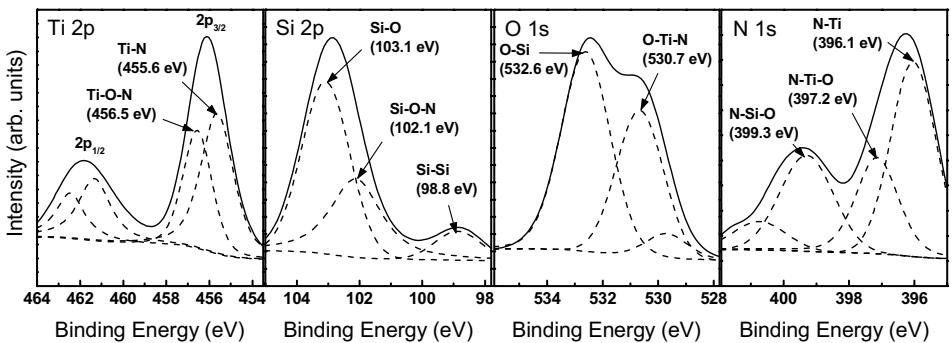
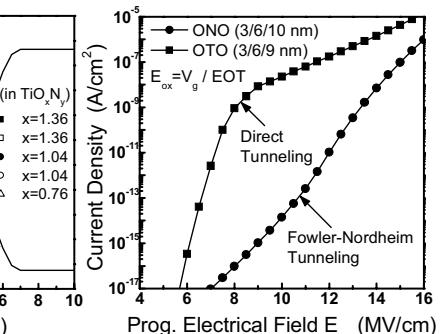
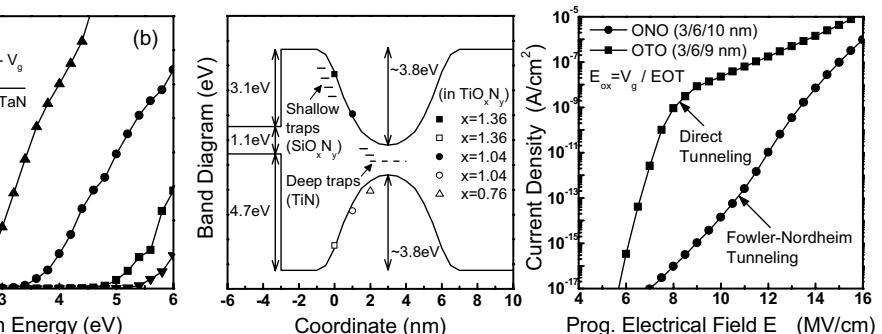
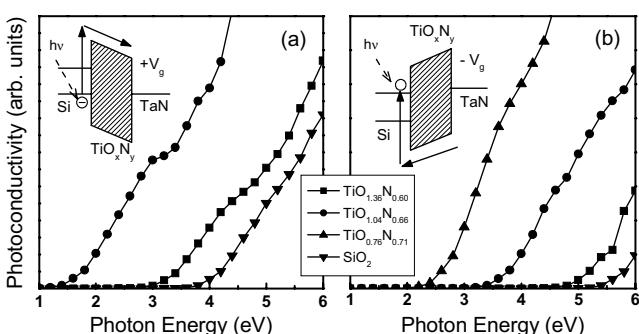


Fig. 6: XRD spectra of reference sample (#1) before and post RTP at vacuum at 900°C for 10s.



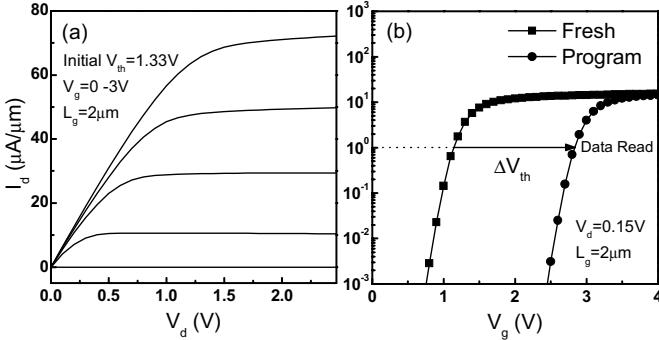


Fig. 10: (a) Good I_d - V_d characteristics of a fresh SOTOT device with a channel length $L_g = 2\mu m$. The initial V_{th} is 1.33V. (b) I_d - V_g characteristics of a SOTOT device before and after program by $E_{ox} = 6\text{MV}/\text{cm}$ for 10^{-3}s . ΔV_{th} is read at $I_d = 1\mu A/\mu m$ by read bias of $V_d = 0.15\text{V}$.

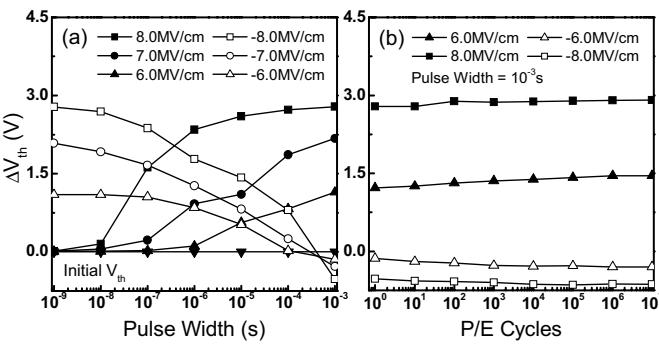


Fig. 12: (a) ΔV_{th} transients of a fresh SOTOT device P/E by $E_{ox} = (\pm)6-8\text{MV}/\text{cm}$ for $10^{-9}-10^{-3}\text{s}$. (b) ΔV_{th} transients of a SOTOT device P/E by $E_{ox} = (\pm)6/8\text{MV}/\text{cm}$ for 10^{-3}s throughout the 10^7 P/E cycles. The ΔV_{th} window increases during the P/E cycling may be induced by trap generation in the SiO_xN_y transition layer.

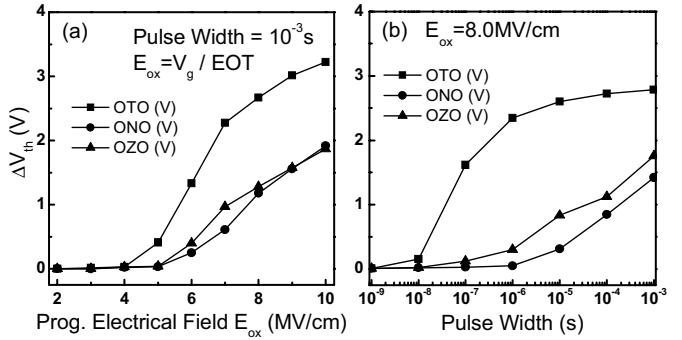


Fig. 11: (a) ΔV_{th} transients of SOTOT (OTO) and SONOS devices with a Si_3N_4 (ONO) and ZrO_2 (OZO) trapping layer induced by $E_{ox} = 4-10\text{MV}/\text{cm}$ for 10^{-3}s . (b) ΔV_{th} transients of various devices induced by $E_{ox} = 8\text{MV}/\text{cm}$ for $10^{-9}-10^{-3}\text{s}$. $\Delta V_{th} = 2.34\text{V}, 0.06\text{V}$, and 0.31V at 10^{-6}s for OTO, ONO, and OZO devices, respectively.

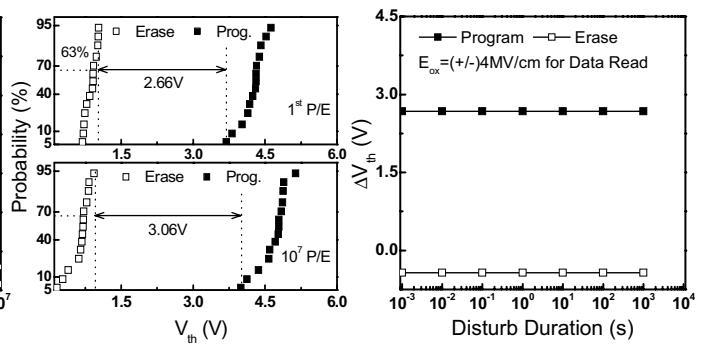


Fig. 13: Cumulative distribution of V_{th} windows of 14 SOTOT devices. $\Delta V_{th} = 2.66\text{V}$ at the 1st P/E cycle and $\Delta V_{th} = 3.06\text{V}$ at the 10^7 P/E cycle.

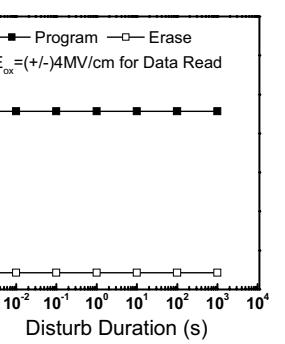


Fig. 14: ΔV_{th} transients disturbed by $E_{ox} = \pm 4\text{MV}/\text{cm}$ for a SOTOT device post the 10^7 P/E cycles at 25°C . ΔV_{th} is $\sim 3.09\text{V}$ for up to 10^3s .

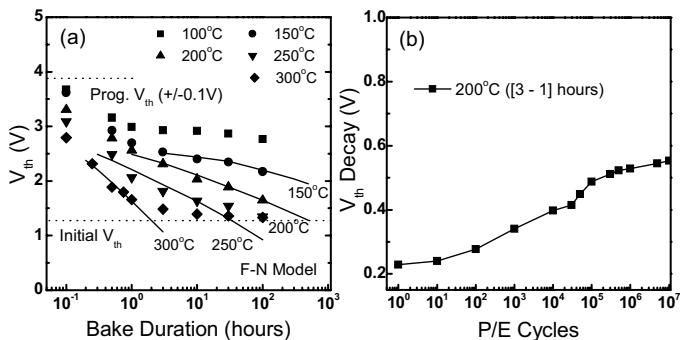


Fig. 15: (a) Accelerated data retention of a fresh SOTOT device at $100^\circ\text{C}-300^\circ\text{C}$ (dots) and the estimated V_{th} decay transients by the F-N model (solid lines) [11]. (b) The V_{th} decays throughout the 10^7 P/E cycles during 200°C baking. The V_{th} decays are extracted between the 3rd/ the 1st hour to avoid the disturbances induced by the SiO_xN_y shallow traps.

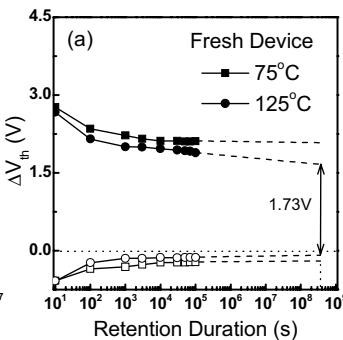


Fig. 16: (a) ΔV_{th} transients of a SOTOT device post the 1st P/E cycle and (b) those post the 10^7 P/E cycles. The extrapolated 10-year V_{th} windows are 2.11V and 1.93V at 75°C , and they are 1.73V and 1.47V at 125°C (a) before and (b) post the 10^7 P/E cycling.

Table 2. Comparison of this work to the other works

References	This work	[2] IEDM 2005 pp.547-550	[3] IEDM 2006 pp.971-974	[4] IEDM 2007 pp.75-78	[8] VTS 2008 4530799	[12] VLSI 2005 pp.122-123	[13] IEDM 2008 pp.223-226
Device structure	SOTOT	SONONOS	SONHAS	SOSONOS	SO(TA)AS	SONOS	(DSSB) SONOS
Layer Thicknesses (nm)	-/3/6/9/-	-/1.5/2/1.8/7/9/-	-/2.6/1.8/16/10.5/-	-/1/1.2/1/4/6.5/-	-/4/0.5-1/20/-	-/4.5/7/4.8/-	-(Si Fin)/3/6/4/-
P/E electrical field (MV/cm)	6-8	10-12	13-15	6.9-7.7	-	(BTBT) 12.3-15.4	(EBEHE) ~ 12
Prog. durations for $\Delta V_{th}=2\text{V}$	$3 \times 10^{-7}\text{s}$	$\sim 7 \times 10^{-5}\text{s}$	$\sim 1 \times 10^{-4}\text{s}$	$\sim 2 \times 10^{-4}\text{s}$	$\sim 1 \times 10^{-3}\text{s}$	$2 \times 10^{-7}\text{s}$	$3 \times 10^{-8}\text{s}$
Erase durations for $\Delta V_{th}=2\text{V}$	$\sim 2 \times 10^{-4}\text{s}$	$\sim 10^{-2}\text{s}$	$\sim 2 \times 10^{-4}\text{s}$	$\sim 2 \times 10^{-4}\text{s}$	$\sim 1 \times 10^{-3}\text{s}$	$1 \times 10^{-6}\text{s}$	$\sim 1 \times 10^{-6}\text{s}$
V_{th} windows (V)	~ 3	~ 6	~ 9	~ 1.8	~ 2.5	~ 6	~ 6
Endurance (P/E cycles)	$>10^7$	$>10^4$	$\sim 10^4$	$>10^5$	$>10^4$	$\sim 10^4$	$>10^5$
10-year V_{th} windows decay (%)	52% at 125°C (post 10^7 cycles)	$\sim 25\%$ at 150°C (post 10^4 cycles)	47% at 150°C (post 10^4 cycles)	50% at 125°C (before cycling)	34% at 25°C (before cycling)	-	41% at 25°C (post 10^3 cycles)