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ARTICLE

1,000,000 On/Off Ratio in Sub-1 nm Channel Length Carbon Nanotube/Monolayer MoS_2/Carbon Nanotube Vertical Transistors

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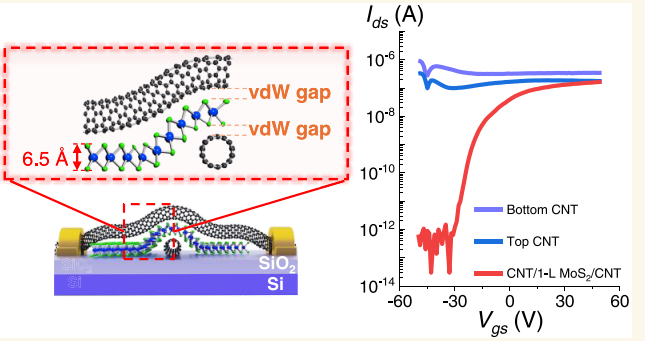
ABSTRACT: **Vertical field effect transistors (VFETs) using graphene and transition metal dichalcogenide (TMD) heterostructures are promising for downsizing the channel length to a monolayer TMD thickness of 0.65 nm. However, graphene/monolayer TMD/metal VFETs struggle with a low on/off ratio due to gate field screening by the graphene layer and a high off-state tunneling current caused by the large contact area. Here, we propose a 0.65 nm channel length VFET with a very high on/off current ratio made by cross-stacking top and bottom carbon nanotubes (CNTs) with a monolayer TMD in between. The ultranarrow junction area in the CNT/monolayer TMD/CNT VFET can significantly reduce the off-state tunneling current. Additionally, the gate field is transmitted from the sidewall of the bottom CNT to the monolayer MoS_2 vertical channel between the two CNTs without field screening, achieving very strong gate modulation. As a result, our devices exhibit about 10^5 times higher on/off ratio (a maximum of 10^6), 10^5 times lower off current (10^{-13} A), and 560 times lower subthreshold swing (SS) (125 mV dec^{-1}) compared to graphene/monolayer TMD/metal VFETs. In the comparison between multilayer MoS_2 and monolayer MoS_2 VFETs, rigid multilayer MoS_2 forms a large air gap at the multilayer MoS_2/CNT/substrate, which reduces electric field transmission. In contrast, monolayer MoS_2 bends significantly along the sidewall of the CNT, resulting in minimal air gap formation and enhancing the electric field effect in the channel. As a result, the CNT/monolayer MoS_2/CNT VFET shows a 10 times higher on-current saturation and on/off ratio compared to the CNT/multilayer MoS_2/CNT VFET.**



KEYWORDS: *transition metal dichalcogenides, carbon nanotube, sub-1 nm channel length, vertical field effect transistor, chemical vapor deposition*

INTRODUCTION

Vertical field effect transistors (VFETs) based on two-dimensional (2D) semiconducting materials have the potential to sustain Moore's law into the future.[1−14] Unlike conventional planar transistors, which are constrained to a channel length of 3 nm due to the resolution limitations of ultraviolet lithography processes,[15] the channel length of VFETs can be scaled down to a limit of 0.65 nm using monolayer transition metal dichalcogenides (m-TMDs).[14] However, challenges arise in fabricating VFETs with sub-1 nm channel lengths using evaporated metal contacts, primarily concerning the metal−semiconductor interface, metal diffusion, and layer damage caused by high-energy atom and atomic cluster bombardment during metal deposition.[16] Significant metal diffusion can enhance the direct tunneling current between the source and drain, leading to reduced on/off ratios and potential device failures due to short circuits.

To address these challenges, VFETs with van der Waals (vdW) heterostructures with sub-5 nm channel lengths have been proposed. This approach aims to improve interface contacts and prevent layer damage during fabrication, with the

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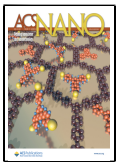

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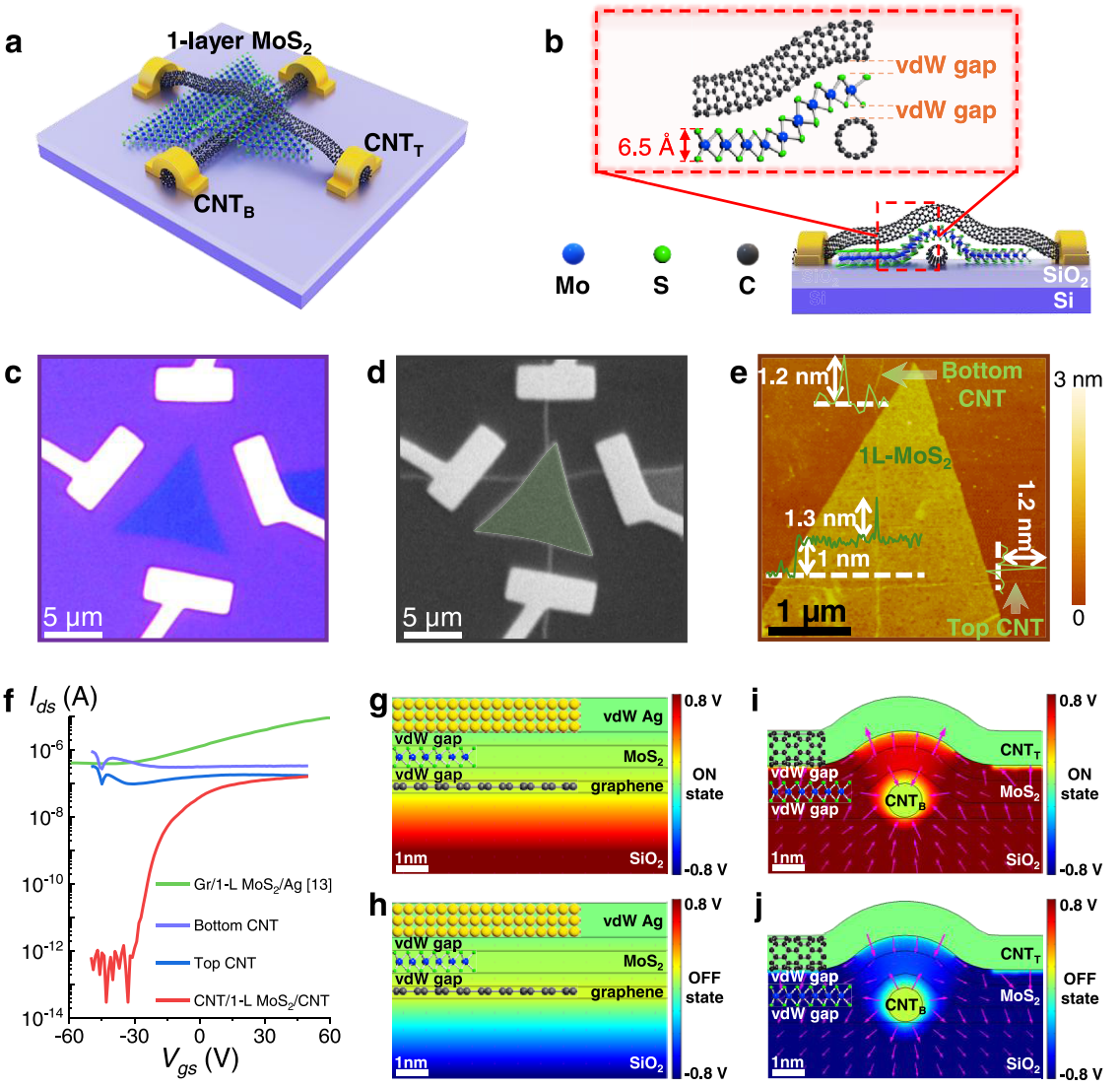

Figure 1. Structural characterization of the C/M/C VFET compared to graphene vdW contacts for the VFETs. (a) 3D schematic of the CNT/monolayer MoS_2/CNT VFET. (b) Cross-sectional schematic of the C/M/C VFET with a monolayer MoS_2 sandwiched between two cross-stacked CNTs. (c) Optical microscope image of the C/M/C VFET. (d) False-colored SEM image of the C/M/C VFET with a monolayer MoS_2 as the channel. Inset: The green color represents a monolayer MoS_2 flake. (e) AFM topography image of the CNT_B/MoS_2/CNT_T heterostructure. Inset: Height profiles of MoS_2, CNT_B, and CNT_T. (f) Transfer characteristics of the C/M/C VFET compared to the graphene/MoS_2/Ag VFET (reproduced with permission from ref 13. Copyright 2021 Springer Nature) at V_{ds} = 0.1 V. (g, h) Electrostatic simulations for the graphene/MoS_2/Ag VFET at V_g = 3 V (on state, (g)) and V_g = −3 V (off state, (h)) with V_{ds} = 0.1 V. (i−j) Electrostatic simulations for the C/M/C VFET at V_g = 3 V (on state, (i)) and V_g = −3 V (off state, (j)) with V_{ds} = 0.1 V. The magenta arrows shown in (g−j) represent the magnitude and direction of the electric field.

semiconductor channel sandwiched between graphene and transferred metal electrodes.[5,9,13,17] However, the presence of the bottom graphene layer significantly screens the gate electric field, resulting in decreased electrostatic modulation of the gate on the TMD monolayer channel and a low on/off ratio of 26 in VFETs.[13,18]

Semimetal carbon nanotubes (CNTs) are emerging as promising candidates for tubular nanoscale wires, particularly when combined with two-dimensional (2D) materials to achieve multifunctionality and miniaturization due to their perfect tubular structure,[19] electrical and thermal stability,[20,21] and high current density.[22] Recently, CNTs have been utilized as electrodes in mixed-dimensional structures with a special emphasis on van der Waals integration. Examples include CNT/self-assembled molecule/CNT ferroelectric memory (1D-0D-1D),[23] CNT with a 1 nm gate length for MoS_2 transistors (1D-2D),[24] single CNT/MoS_2/Au vertical transistors (1D-2D-3D),[12] CNT network/MoS_2/Au vertical transistors (1D-2D-3D),[18] CNT/MoS_2/CNT planar transistors,[25] CNT/19 nm MoS_2/CNT vertical transistors (1D-2D-1D),[8] and CNT/16 nm WSe_2/14 nm MoS_2/CNT p−n heterojunction photodetectors.[26] By stacking semimetal/semiconductor van der Waals contacts, it is possible to suppress metal-induced gap states (MIGS) and avoid Fermi-level pinning.[27,28] Moreover, the density of states (DOS) of CNTs is close to the Dirac point and low between the first van Hove singularities.[29] This characteristic allows for efficient gate-controlled modulation of the Fermi level through an external gate potential. Thus, individual CNTs present an excellent

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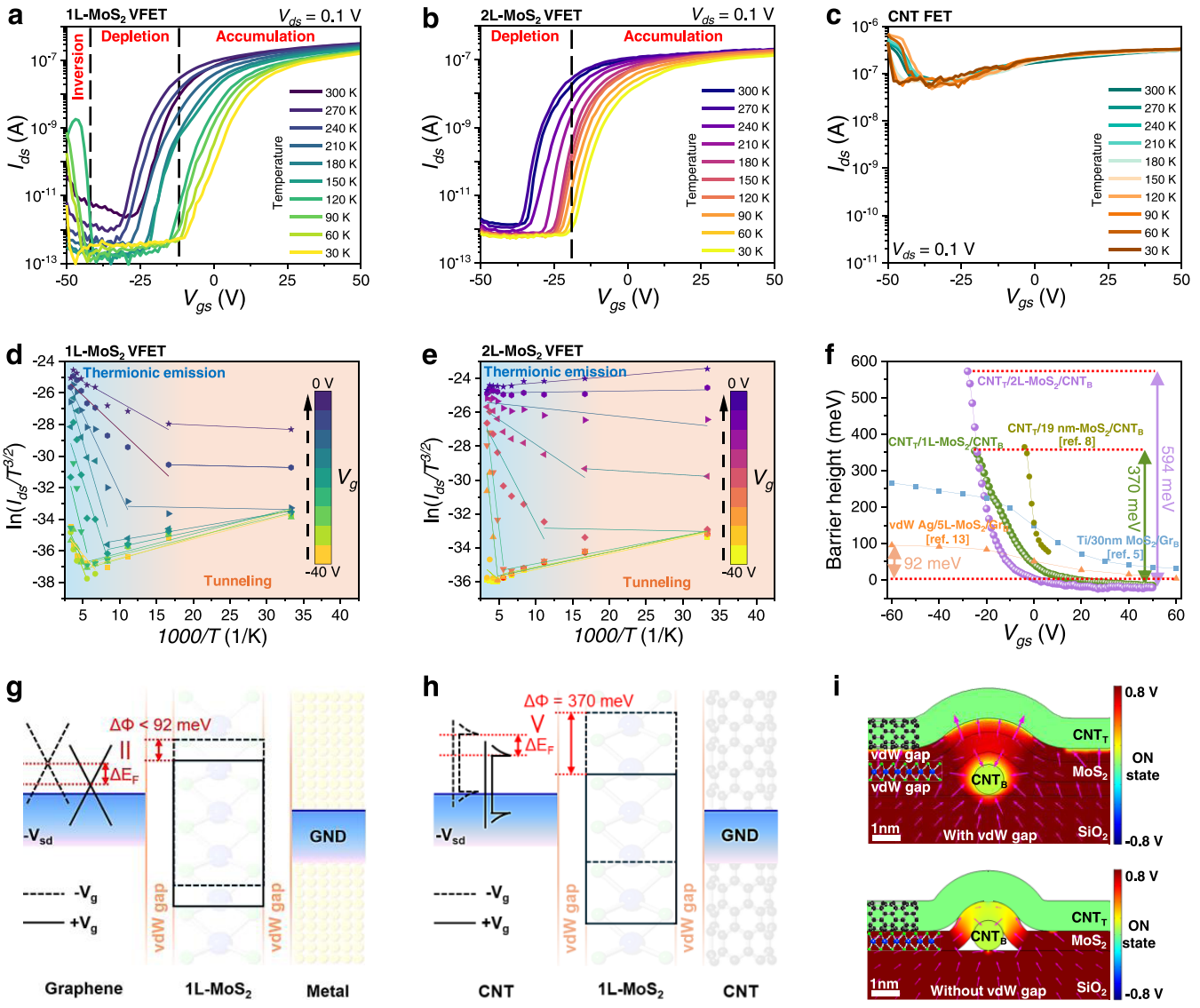

Figure 2. Electrical transport measurements are dependent on temperature. (a–c) Transfer characteristics of the 1L-MoS_2 C/M/C VFET (a), 2L-MoS_2 C/M/C VFET (b), and CNT planar FET (c) at V_{ds} = 0.1 V under different temperatures. (d, e) Arrhenius plots of two individual CNTs sandwiching a monolayer MoS_2 (d) and a bilayer MoS_2 (e). (f) Gate-dependent BH of the 1L-MoS_2 and 2L-MoS_2 C/M/C VFET compared to the graphene/30 nm MoS_2/Ti VFET (Reproduced with permission from ref 5. Copyright 2013 Springer Nature), graphene/5-layer MoS_2/vdW Ag VFET (reproduced with permission from ref 13. Copyright 2021 Springer Nature), and CNT/19 nm MoS_2/CNT VFET (reproduced with permission from ref 8. Copyright 2017 John Wiley & Sons, Inc.). (g, h) Energy band diagram of graphene/1-layer MoS_2/metal (g) and CNT/1-layer MoS_2/CNT (h) heterostructures. ΔE_F and $\Delta\Phi$ represent the difference in Fermi levels and barrier heights under negative and positive gate voltages. (i) Electrostatic simulations for CNT/1L-MoS_2/CNT VFETs with (top panel) and without vdW gaps (bottom panel) at V_g = 3 V and V_{ds} = 0.1 V.

alternative to graphene and metal electrodes for achieving the ultimate contact scaling in 2D nanodevices.

In this work, we propose a CNT/monolayer TMD/CNT (C/M/C) vdW vertical heterostructure to minimize the limitations of VFETs and prevent the tunneling current-induced short-circuit. The structure of the C/M/C VFET is demonstrated with monolayer MoS_2, WSe_2, and $MoSe_2$ sandwiched between cross-stacked CNTs. The screening effect in the C/M/C structure is significantly reduced by transmitting the gate field from the sidewall of the bottom CNT to the vertical channel of monolayer MoS_2, allowing for direct modulation of the MoS_2 energy band. The ultranarrow junction area in the C/M/C VFET also reduces the off-state tunneling current. The CNT/MoS_2/CNT junction demonstrates a large barrier height (BH) change of 370 meV, which is significantly greater than the E_F shift (20 meV with V_g = −30–20 V) of semimetallic CNTs. In contrast, the graphene/MoS_2 junction shows a smaller BH change (<92 meV) depending on the E_F shift of graphene. Consequently, our C/M/C VFETs exhibit on/off ratios for VFETs with monolayer MoS_2 (10^5–10^6), bilayer MoS_2 (10^5–10^6), monolayer WSe_2 (10^4), and monolayer $MoSe_2$ (10^3) at room temperature. The subthreshold swing (SS) further improved with a decrease in the gate dielectric thickness from 300 nm SiO_2 (5 V dec^{-1}) to 5.5 nm h-BN (125 mV dec^{-1}). The monolayer C/M/C VFETs demonstrate even better electrical performance than the multilayer C/M/C VFETs. The rigid structure of multilayer MoS_2 creates a substantial air gap at the multilayer MoS_2/

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CNT/substrate heterostructure, diminishing the transmission of the electric field. In contrast, monolayer MoS_2 bends significantly along the sidewall of the CNT, resulting in minimal air gap formation and, thus, enhancing the electric field effect within the channel. As a result, the monolayer C/M/C VFET shows a higher on/off ratio of 10^6 and on-current saturation at 10^{-7} A compared to the multilayer C/M/C VFET (on/off ratio of 10^5 and on-current saturation at 10^{-8} A).

RESULTS AND DISCUSSION

Semimetal CNT-Sandwiched vdW Vertical Heterostructures for VFETs. Figure 1a shows the VFET configuration of a CNT/monolayer-MoS_2/CNT heterostructure (C/M/C) on the SiO_2/Si substrate. An overview of the fabrication process is provided in Figure S1 (Supporting Information). Briefly, the bottom CNT (CNT_B) was initially grown by using the chemical vapor deposition (CVD) technique and transferred to a silicon wafer coated with 300 nm SiO_2. Monolayer MoS_2 was synthesized by CVD and transferred onto CNT_B. Next, the top CNT (CNT_T) was cross-stacked on the CNT_B/MoS_2 heterostructure. The metal electrodes were patterned on CNT_B and CNT_T using electron-beam lithography and deposited with Cr/Au (5/50 nm) through electron-beam deposition.

Figure 1b exhibits the cross-sectional schematic of the C/M/C VFET, featuring vdW gaps formed from the physical stacking of the heterostructure with a channel length of 0.65 nm. Figure 1c displays an optical microscopy image of the C/M/C VFET, in which a grown monolayer MoS_2 flake is transferred onto CNT_B, and CNT_T is aligned perpendicularly to CNT_B. The presence of CNT_T and CNT_B can be confirmed by a scanning electron microscopy (SEM) image of the C/M/C VFET, as shown in Figure 1d. Figure 1e exhibits an atomic force microscopy (AFM) topography image and height profile distribution of the C/M/C, revealing a clean surface of the CNT, MoS_2, and the heterojunction, confirming a monolayer MoS_2 and a CNT thickness of 1.2 nm used in the C/M/C VFET. The Raman spectra of the CNT and monolayer MoS_2 on a Si/SiO_2 substrate are shown in Figure S2 (Supporting Information).

Figures 1f and S3 present the transfer characteristics of the top CNT, bottom CNT, and C/M/C VFET. The top and bottom CNT electrodes exhibit metallic behavior with no gate modulation, indicating that the gate modulation of the C/M/C VFET occurs only in the vertical monolayer MoS_2 channel. The C/M/C VFET shows an ultrahigh on/off ratio of 10^6, significantly higher than the previous graphene/monolayer MoS_2/metal VFET, which had an on/off ratio of 26.[13] However, the off-state tunneling current increases proportionally with increasing V_{ds} and causes the degradation of the on/off ratio (Figure S4, Supporting Information). We also measured the graphene/monolayer MoS_2/graphene heterostructure VFET (Figure S5, Supporting Information), showing a very small on/off ratio of 1.2. Notably, the large contact area of graphene/MoS_2/metal and graphene/MoS_2/graphene VFETs increases the off-state tunneling current to 10^{-7} A,[5,13] while the ultranarrow contact area in our C/M/C VFETs can significantly reduce the off-state tunneling current to 10^{-13} A. The simulated electrical characteristics are employed to confirm that the ultranarrow junction area can significantly reduce the off-state tunneling current (Figure S6, Supporting Information). The ideal G/1L-M/G VFET exhibits a significantly higher tunneling current (10^{-1} A μm^{-2}) than the real device (10^{-6} A μm^{-2}) due to the absence of contamination and the van der Waals gap in the ideal case. By normalizing the tunneling current to the VFET device area, we can extract the tunneling current for a given VFET device area (blue dashed line in Figure S6b).

To investigate the high on/off ratio in the C/M/C VFET compared to the previous graphene/monolayer MoS_2/metal structure, the electrostatic potential of each device was simulated using a finite-element method conducted with COMSOL Multiphysics software (Figure 1g–j). The model parameters are listed in Table S1 (Supporting Information). In the electrostatic potential of graphene/monolayer MoS_2/metal of the previous structure (Figure 1g,h), the gate electric field is mostly blocked by the graphene layer, and only a partial gate field is transmitted to the monolayer MoS_2. In the C/M/C VFET (Figure 1i,j), in contrast, the gate electric field is transmitted from the sidewall of CNT_B to the monolayer MoS_2 between the two CNTs without any field screening. Therefore, very strong gate modulation is achieved in the vertical C/M/C configuration. Such strong gate modulation in the C/M/C VFET is consistently observed in eight C/M/C VFETs with a maximum on/off ratio of 1.01×10^6 (Figure S7, Supporting Information).

Barrier Height Profile of C/M/C VFETs under Gate Modulation. To investigate the gate modulation of the C/M/C VFET, we measured temperature-dependent electrical characteristics of the C/M/C VFET. For the monolayer MoS_2 C/M/C VFET (1L-MoS_2 VFET), as the temperature decreases, the thermal activation of carriers in MoS_2 is suppressed, decreasing the off current of the 1L-MoS_2 VFET (Figures 2a and S8–S9, Supporting Information). With the excellent gate modulation of the 1L-MoS_2 VFET, hole carrier inversion is observed in the negative gate region.[30] When increasing the channel thickness to bilayer MoS_2 for the 2L-MoS_2 VFET (Figures S10–S11, Supporting Information), the 2L-MoS_2 VFET reduces the probability of carrier tunneling through the larger barrier, resulting in a reduced variation in the off-current state of transfer characteristics at low temperatures (Figures 2b and S12–S13, Supporting Information). The electrical characteristics of CNTs used as electrodes show negligible change at low temperatures (Figures 2c and S14, Supporting Information).

From the temperature-dependent studies, we have determined the BH (Φ_B) across the junctions of CNT-MoS_2. According to the thermionic emission theory, Φ_B at the CNT/MoS_2 interfaces (Figure 2d,e) can be determined by the slopes of $\ln(I_{ds}/T^{3/2})$ against q/kT for V_g from the Arrhenius plot,[31] where I_{ds} is the drain-to-source current, T is the temperature, q is the elementary charge, and k is the Boltzmann constant. Figure 2f shows the derived BH from Figure 2d,e. The BH modulations ($\Delta\Phi_B$) at the CNT/monolayer MoS_2 and CNT/bilayer MoS_2 junctions exhibit 370 and 594 meV, which are higher than those observed in graphene/30 nm MoS_2 [ref 5] ($\Delta\Phi_B$ = 234 meV), graphene/5-layer MoS_2 [ref 13] ($\Delta\Phi_B$ = 92 meV) junctions, and CNT/19 nm MoS_2/CNT VFET [ref 8] ($\Delta\Phi_B$ = 286 meV) junctions with the on-state BH saturated at 77 meV near a 6 V gate bias. It is noted that the difference in off-state barrier heights between 1L-MoS_2 and 2L-MoS_2 VFETs arises because the off-state barrier of the 1L-MoS_2 VFET (354 meV) is not sufficiently high to block thermally excited electrons, whereas the higher barrier of the 2L-MoS_2 VFET (573 meV) effectively suppresses the thermally activated carrier transport. The BH modulation of monolayer MoS_2

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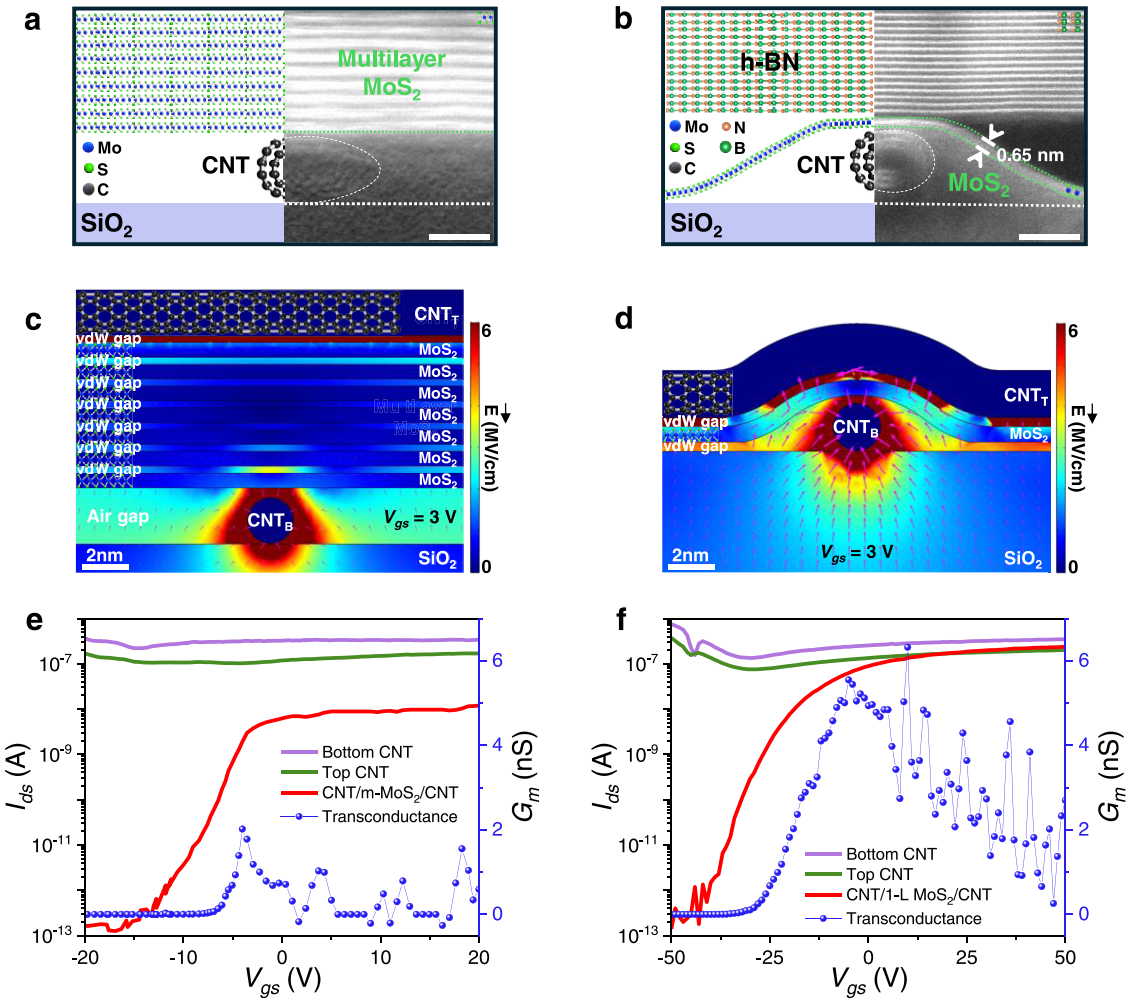

Figure 3. Comparison of multilayer and monolayer MoS_2 stacked on CNTs for VFETs. (a, b) Cross-sectional STEM image of multilayer MoS_2 (a) and monolayer MoS_2 (b) stacked on individual CNTs forming a vdW gap of 0.35 nm. (c, d) Electric field (E) contour plots of CNT_B/multilayer MoS_2/CNT_T (c) and CNT_B/monolayer MoS_2/CNT_T (d) VFETs in the on state (V_g = 3 V and V_{ds} = 0.1 V). (e) Transfer curve (red line), transconductance (blue line) of the CNT_B/multilayer MoS_2/CNT_T VFET, and the transfer curve of bottom CNT (purple line) and top CNT FETs (green line) at V_{ds} = 0.1 V (reproduced with permission from ref 8. Copyright 2017 John Wiley & Sons, Inc.). (f) Transfer curve (red line), transconductance (blue line) of the CNT_B/monolayer MoS_2/CNT_T VFET, and the transfer curve of bottom CNT (purple line) and top CNT FETs (green line) at V_{ds} = 0.1 V.

VFETs should be lower than that of five-layer MoS_2 due to the lower on/off ratio, although this has not been shown in previous studies. Furthermore, the CNT/MoS_2 junction exhibits sharp BH modulation within V_g = -20 − 0 V, whereas the graphene/MoS_2 junction is modulated over a wide gate range of V_g = -60 − 20 V.

The energy band diagrams of graphene/MoS_2/metal and CNT/MoS_2/CNT junctions are drawn based on the BH profiles (Figure 2g,h). In the graphene/MoS_2/metal junction, the strong screening effect of graphene blocks the gate field, so the BH change of the graphene/MoS_2 junction is fully dependent on the Fermi level (E_F) shift of graphene by V_g modulation, resulting in a small BH change. In contrast, the CNT/MoS_2/CNT junction exhibits a very large BH change of 370 meV, which is larger than the typical E_F shift (20 meV with V_g = -30 − 20 V) of semimetallic CNTs.[32] It is because the gate field is effectively transmitted from the sidewall of CNT_B to the monolayer-MoS_2 vertical channel between the two CNTs without the field screening and directly modulates MoS_2 E_F. It is noted that the vdW gap between MoS_2 and CNTs plays an important role in the large gate modulation.

Figure 2i shows the electrostatic potential simulation results with (top) and without the vdW gap (bottom panel). The gate modulation of the C/M/C VFET without the vdW gap shows a very small potential change at the CNT/MoS_2/CNT vertical junction due to the Fermi level pinning effect by metal-induced gap states (MIGS). On the other hand, the C/M/C VFET with the vdW gap can significantly reduce MIGS and Fermi level blocking effects.

Comparison between Multilayer and Monolayer MoS_2 in C/M/C VFETs. The difference in shape between multilayer MoS_2 and monolayer MoS_2 stacked on CNTs arises from their distinct structural and mechanical properties, which play a critical role in device performance. The cross-sectional scanning transmission electron microscopy (STEM) images provide clear evidence of the differences between the CNT−multilayer MoS_2 interface and the CNT−monolayer MoS_2 interface, as shown in Figure 3a,b, respectively. STEM/energy-dispersive spectroscopy (STEM-EDS) mapping of the CNT−multilayer MoS_2 and CNT−monolayer MoS_2 interfaces confirms the distribution of the main elements C, Mo, and S, as presented in Figures S15−S16 (Supporting Information),

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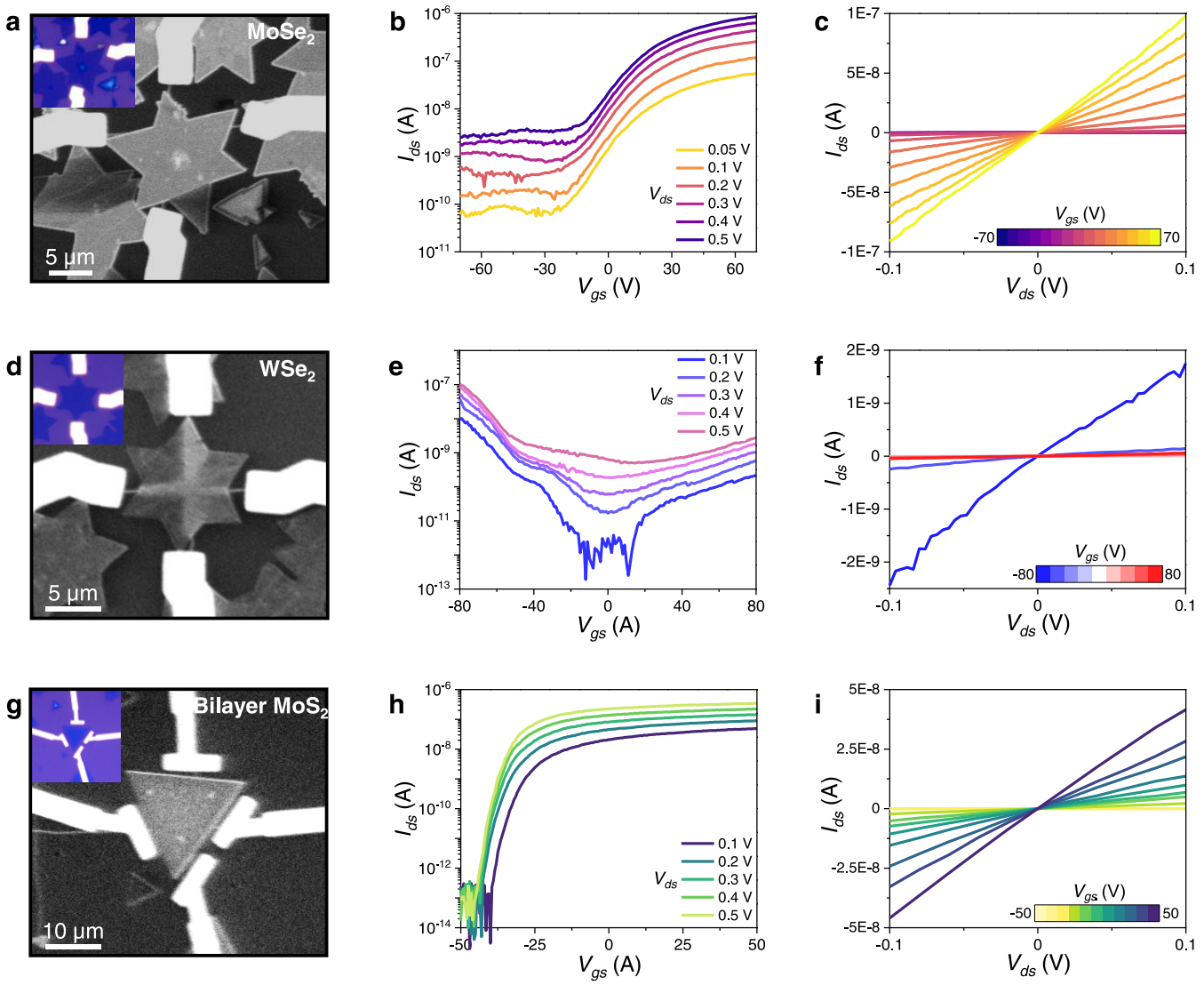

Figure 4. C/M/C VFETs based on monolayer $MoSe_2$, monolayer WSe_2, and bilayer MoS_2 channel lengths. (a, d, g) SEM images of monolayer $MoSe_2$ (a), monolayer WSe_2 C/M/C (d), and MoS_2 (g) C/M/C VFETs, with OM images of the devices shown in the inset. (b, e, h) Transfer curves of monolayer $MoSe_2$ (b), monolayer WSe_2 (e), and bilayer MoS_2 (h) C/M/C VFETs at room temperature. (c, f, i) Output curves of monolayer $MoSe_2$ (c), monolayer WSe_2 (f), and bilayer MoS_2 (i) C/M/C VFETs at room temperature.

respectively. When multilayer MoS_2 is stacked on a CNT, it tends to exhibit flat layers because the vdW bonding of each layer in multilayer MoS_2 leads to a rigid and stable structure without significant interlayer distortion. Such rigid multilayer MoS_2 forms a large air gap between the multilayer MoS_2 and the substrate when the CNT is sandwiched between them. In contrast, monolayer MoS_2, with its flexible and atomically thin structure, bends significantly when stacked on the CNT. This bending reduces the air gap between monolayer MoS_2 and the substrate, which is expected to enhance the electric field effect in the channel.

To clarify the impact of the air gap on device performance, the electric field distribution is simulated for both the multilayer C/M/C VFET and monolayer C/M/C VFET at V_g = 3 V and V_{ds} = 0.1 V (at CNT_B), as shown in Figure 3c,d, respectively. The electric field is significantly reduced in the air gap of the multilayer C/M/C VFET, while it retains its strength through the narrow vdW gap in the monolayer C/M/C VFET. Additionally, it is observed that the electric field in the multilayer C/M/C VFET gradually decreases across the vdW gaps between the MoS_2 layers. This reduction in the electric field within the multilayer C/M/C VFET weakens the gate modulation of the MoS_2 channel. As a result, the multilayer C/M/C VFET exhibits an on/off ratio of 10^5 with limited on-current saturation of 10^{-8} A (Figure 3e),[8] while the monolayer C/M/C VFET shows a higher on/off ratio of 10^6 and on-current saturation at 10^{-7} A (Figure 3f) limited by the current of CNT in comparison to the multilayer C/M/C VFET. Besides, the transconductance (G_m) of the monolayer C/M/C VFET is three times larger than that of the multilayer C/M/C VFET, indicating that the gate voltage can more effectively modulate the monolayer MoS_2 channel.

Various Monolayer Semiconductor Materials in C/M/C VFETs. Benefiting from the C/M/C VFETs, chemical vapor deposition (CVD)-grown monolayer $MoSe_2$ and WSe_2 are employed to integrate with CNT electrodes for ultrashort-channel C/M/C VFETs. Figure 4a,d shows optical and SEM images of C/M/C VFETs for monolayer WSe_2 and $MoSe_2$ channel lengths, respectively. Raman, photoluminescence (PL), and atomic force microscopy (AFM) measurements

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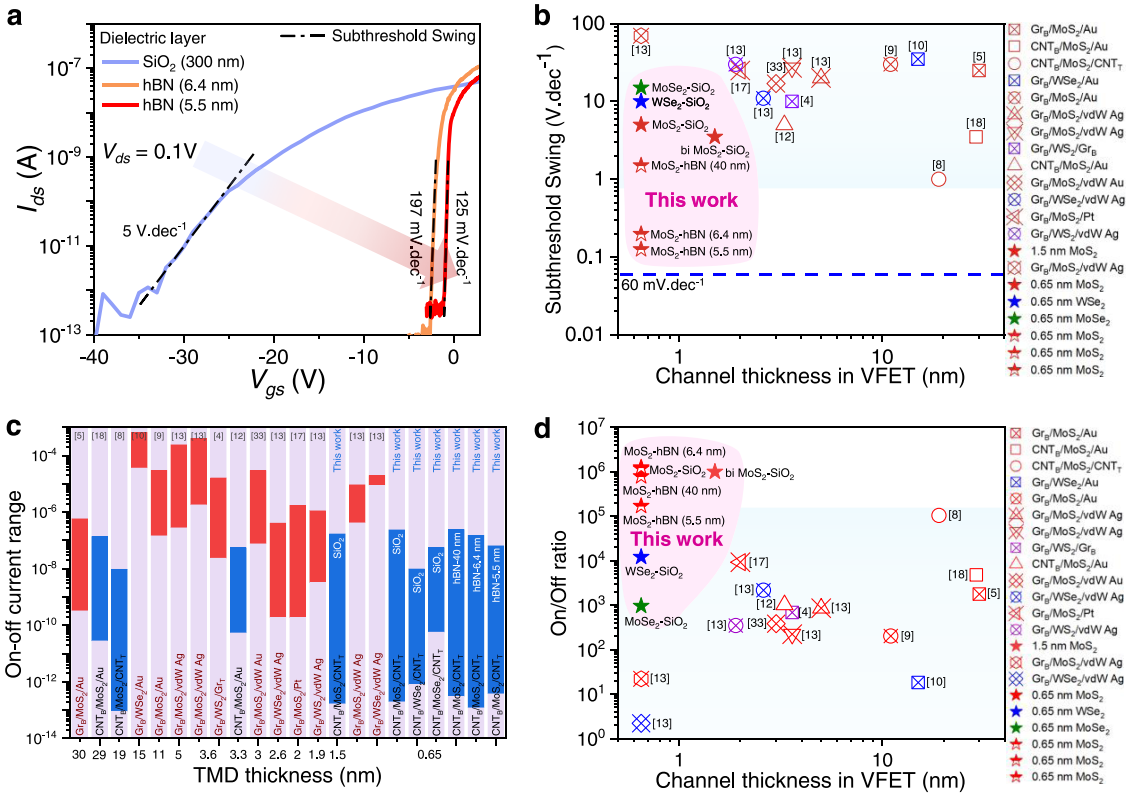

Figure 5. Performance comparison of C/M/C VFETs with other VFETs. (a) Transfer characteristics of C/M/C VFETs using MoS_2 channels with different h-BN dielectrics of 6.4 and 5.5 nm and a SiO_2 dielectric of 300 nm at V_{ds} = 0.1 V. The dashed lines represent the SS. (b) Benchmarking the SS along the channel length in VFETs (red: MoS_2, blue: WSe_2, purple: WS_2, green: $MoSe_2$). (c) Comparison of the on/off ratio of our C/M/C VFETs of monolayer MoS_2, $MoSe_2$, and WSe_2 and bilayer MoS_2 with other VFETs. Note: VFETs use the bottom CNT (blue color) and the bottom graphene (red color) as the bottom electrode. (d) Benchmarking the on/off ratio along the channel length in VFETs (red: MoS_2, blue: WSe_2, purple: WS_2, green: $MoSe_2$). All reference values are shown in Table S2 (Supporting Information).

are utilized to confirm the structural characterization of WSe_2 and $MoSe_2$ C/M/C VFETs, as shown in Figures S17−S18 (Supporting Information). The transfer curves and output curves of $MoSe_2$ (Figure 4b,c) and WSe_2 C/M/C VFETs (Figure 4e,f) show high on/off ratios of 10^3 and 10^4 at room temperature, respectively. Other devices consistently exhibit the same performance, as shown in Figure S19 (Supporting Information). Additionally, the channel length increases from monolayer (0.65 nm) to bilayer (1.5 nm), as illustrated in OM and SEM images of the 2L-MoS_2 C/M/C VFET in Figure 4g. The transfer and output curves clearly show the improved suppression of the off-state current under high V_{ds}, indicating effective mitigation of the drain-induced tunneling current (Figure 4h,i). Additional devices consistently exhibit high performance with on/off ratios of approximately 10^6, as shown in Figure S20 (Supporting Information).

Performance Comparison of C/M/C VFETs with Other VFETs. To enhance the device performance, we used the thin h-BN layer as a gate insulator (Figures 5a and S21, Supporting Information). The transfer curve of the C/M/C VFET with a 300 nm SiO_2 gate insulator shows a subthreshold swing (SS) of 5 V dec^{-1} and V_{th} of −28 V. Using a 40 nm h-BN dielectric in the C/M/C VFET significantly reduces the SS to 1.5 V dec^{-1} and V_{th} to −9 V. Further decreasing the h-BN thickness to 6.4 and 5.5 nm results in an SS of 197 and 125 mV dec^{-1} with V_{th} of −2.5 and −0.9 V, respectively. Figure 5b and Table S2 (Supporting Information) show the SS comparison of C/M/C VFETs with other VFETs.[4,5,8−10,12,13,17,18,33] Our C/M/C VFETs with 5.5 nm h-BN achieve 560 times lower SS than that of the previous monolayer MoS_2 VFET (70 V dec^{-1}).[13] Furthermore, we demonstrate monolayer $MoSe_2$ and WSe_2 C/M/C VFETs for the first time, which exhibit similar SS on a SiO_2 dielectric as multilayer WSe_2.[13] Figure 5c,d and Table S2 (Supporting Information) compare the on/off ratio in VFETs with the reduction of channel length thickness.[4,5,8−10,12,13,17,18,33] The graphene/MoS_2/metal and graphene/MoS_2/graphene VFETs generally exhibit a low on/off ratio due to gate field screening by the graphene layer, and the off-state tunneling current increases with decreasing TMD thickness. In contrast, C/M/C VFETs exhibit a high on/off ratio and low off-state tunneling current in overall TMD thicknesses because of the direct gate field modulation to the vertical channel and the ultranarrow vertical contact area.

CONCLUSIONS

In summary, we have successfully demonstrated a CNT/monolayer TMD/CNT van der Waals vertical heterostructure as a promising solution to enhance the performance of VFETs. Our findings show that this configuration not only mitigates the inherent limitations faced by traditional VFETs but also provides significant advantages in terms of electrical performance. The ultranarrow junction area in the C/M/C structure effectively reduces off-state tunneling currents. Furthermore, the gate field is transmitted from the sidewall of the bottom CNT to the vertical TMD channel without screening. This leads to a remarkable on/off ratio of 10^6 for monolayer MoS_2 and even 10^4 for monolayer WSe_2 and $MoSe_2$ at room

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temperature. Moreover, the implementation of thin h-BN as a gate insulator has further improved the subthreshold swing, demonstrating the potential for scaling down 2D transistors effectively. Our research lays a solid foundation for future investigations into the scaling and optimization of ultrathin VFETs, paving the way for next-generation electronic devices and maintaining the momentum of Moore's law.

METHODS

Synthesis of Aligned CNTs. The aligned CNTs are synthesized by CVD using the C precursor from methane gas (99,99% purity). A mixed solution of alumina (Al_2O_3) nanoparticles, bis(acetylacetonato)dioxo-molybdenum ($MoO_2(acac)_2$, 99.98%, Aldrich), poly(vinylpyrrolidone) (M_w 50,000, Aldrich), ($Fe(NO_3)_3{\cdot}9H_2O$, 99.99%, Aldrich), and IPA in deionized (DI) water is sonicated for 1 h. Next, one edge of a SiO_2/Si substrate is dipped in the catalyst solution and dried at 110 °C. The substrate is put in the center of a quartz tube and the growth occurs at 1000 °C with a gas ratio of CH_4/H_2 (10/20 sccm) for 40 min. After completion, argon gas is flowed, and the chamber is naturally cooled to room temperature.

Synthesis of Monolayer and Bilayer MoS_2. Ammonium heptamolybdate (AHM, Sigma-Aldrich) as the Mo source was dissolved in DI water with an opti solution at a ratio of 0.5/0.5/3 (Mo/Opti/H_2O). The catalyst solution was spin-coated on a SiO_2/Si substrate and annealed at 500 °C to remove carbon from opti. Then, the substrate was located in the center of the quartz tube, and the sulfur (S) powder was in the upstream zone. For the growth of monolayer and bilayer MoS_2, 600 mg and 1.5 g of S were melted at 200 °C at the S zone, while the reaction occurred at 800 °C with the flow of 100 sccm N_2 for 5 and 6 min, respectively. After completion, the chamber was cooled to room temperature.

Synthesis of Monolayer WSe_2. Ammonium metatungstate (AMT) hydrate as the W precursor with NaOH powder and opti was dissolved in DI water at a ratio of 0.5/1/0.5 (W/NaOH/Opti). After the catalyst solution was spin-coated and annealed on the substrate, it was located in the middle of the tube, and the Se powder source was in an upstream region. For growth, the temperature was increased to 850 °C with a mixed gas of 300/30 sccm (N_2/H_2), and the reaction occurred in 5 min. After completion, the chamber was cooled to room temperature.

Synthesis of Monolayer $MoSe_2$. Ammonium heptamolybdate (AHM, Sigma-Aldrich) was used as the Mo source. The preparation process was the same as that used for the growth of MoS_2. However, Se powder was used to grow monolayer $MoSe_2$ flakes. For growth, the temperature was up to 850 °C with a gas ratio of 300/30 sccm (N_2/H_2), and the reaction took place for 4 min. After completion, the chamber was cooled to room temperature.

Device Fabrication. The aligned CNT_B on the SiO_2/Si substrate was coated with a PMMA solution and dried at 110 °C for 1 min. Then, the sample was floated on a 2% HF in a DI water mixture to separate the PMMA/CNT_B film from the substrate due to the SiO_2 being etched. The PMMA/CNT_B film was transferred to DI water to remove the HF solution and transferred onto a prime SiO_2/Si substrate. The PMMA film was removed in acetone for 20 min. TMD flakes were transferred on the $CNT_B/SiO_2/Si$ substrate by the wet transfer method, analogous to the procedure for CNT_B transfer. The samples were annealed at 200 °C for 3 h under vacuum with 200 sccm of N_2 to eliminate the bubbles between the heterointerfaces. The aligned CNT_T was dry-transferred on the TMD/$CNT_B/SiO_2/Si$ substrate. The aligned CNT_T was detached from the original substrate with the same method of transferring the aligned CNT_B. The PET substrate was used to flip up the PMMA/CNT_T film. Then, aligned CNT_T was cross-aligned on top of the TMD/CNT_B heterostructure. Lastly, the PMMA film was removed with acetone. The electrodes were patterned on CNTs by EBL and deposited for Cr/Au (5/50 nm) by an EBV system. The useless CNTs were etched by a reactive-ion etching system with 30 sccm O_2 gas.

Measurements. SEM images were taken on a JEOL, JSM-6510 instrument with an accelerating voltage of 1 kV. Raman and PL spectra were obtained on an NTEGRA Spectra system at a 532 nm focused laser. The AFM was performed on a Park NX10, Park system. HR-STEM and EDS mapping were acquired on a JEM-ARM300CF, JEOL, Japan at 300 keV. Electrical measurements were measured on Keithley 4200 under low vacuum (2×10^{-2} Torr) and on a closed-cycle refrigerator system at a low temperature under high vacuum (10^{-7} Torr).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.5c04746.

Characterization of C/M/C heterostructures; electrical characterization of C/M/C VFETs; simulated electrical characteristics of C/M/C VFETs; temperature-dependent $I-V$ characteristics; cross-sectional HRTEM micrographs of MoS_2; AFM of C/M/C VFETs, top-gate electrical characteristics, and table comparison (PDF)

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Author Contributions

W.J.Y. and V.D.D. conceived the research. W.J.Y. and V.D.D. designed the experiment. V.D.D. performed the device fabrication, growth of CNTs and MoS_2, COMSOL Multiphysics simulations, characterization, and data analysis. N.T.D. and S.C.L. contributed to the low-temperature measurement, V.T.V. and M.C.N. performed the growth of $MoSe_2$ and WSe_2, V.K.D. and H.P.D. contributed to the device fabrication, D.P.D., A.C., and H.L. contributed to the data analysis, T.L.P. contributed to the growth of CNTs, and H.W.J. contributed to the simulation. The paper was written by V.D.D. and W.J.Y. with contributions from all the coauthors.

Notes

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The authors declare no competing financial interest.

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